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Optimizing the controller IC for micro HDD process based on Taguchi methods

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Abstract

The future trend of controller integrated circuit (IC) for micro hard disk driver (HDD) is to be lighter, thinner, shorter and smaller. The storage capacity and unit cost of micro HDD is lower than of flash memory card. The optimal packaging manufacturing process for driver IC for micro HDD is Chip Scale Package (CSP). However, the production and assemble process for CSP is much more difficult. Especially, the warpage problem on modeling results in non-conforming products. This research is to discover the optimal production levels for control factors based on the orthogonal array in Tachugi method. The product size used in the study is the driver IC package overall height less than 0.65 mm for micro HDD with CSP manufacturing process.
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1. Introduction

The trend of electronic products is to be thinner, smaller and low profile. With the rapid growth of market demand on DVD player, MP3 and PDA, the demand on gigabyte capacity of multimedia data storage is increasing. Currently, micro Hard Disk Driver (micro HDD) and Flash Memory card are the main products of multimedia data storage. The storage capacities of Flash Memory card are around 16 MB–4 GB, whereas the storage capacities of micro HDD are around 1–80 GB. In addition, the unit production cost per megabyte of micro HDD is much cheaper than that of Flash Memory card. Companies such as Toshiba, Hitachi GST, Cornice and GS Magicstor have shown that high capacity small form factor hard disk drives are possible. In fact the Cornice 25 mm (the so-called 1 in. form factor) storage element has capacities up to 2 GB and sells for less than US $60 [1].

Driver IC is the key electronic component of micro HDD. Driver IC functions as anti-mechanical shock and read head control, and driver IC is responsible of the performance and effectiveness of micro HDD. To satisfy the design of thinner, smaller and low profile of micro HDD, the vertical dimension of driver IC becomes thinner and thinner. In general, the package of driver IC is to protect the components not be affected by the outer environment and to enhance the product reliability of long time usage. However, compared with the normal IC package, it is better to use a Chip Scale Package (CSP) to meet the design of thinner, smaller

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and low profile for portable device [2]. The accepted definition of a CSP is a package that has dimension not larger than 20% of the device [4]. In fact, the ratio of chip area to package area is more than 1.14 when CSP is applied. The ratio approaches the ideal situation of 1. The final package size is about one-third of normal Ball Grid Array (BGA) and the storage capacity can be increased to three times for the same package size. Besides, the central lead of chip by CSP package reduces the transfer distance of signal, minimizes the attenuation, and enhances the anti-interference of chips effectively. The retrieve and storage time of CSP is 15–20% less than the time needed of BGA. However, the CSP assembly process is more difficult than normal IC on the reliability issues [3], especially the changes on stress and strain on CSP assembly when the temperature changes. This change will result in warpage of the components or destroy the shape of the components and finally deteriorate the quality of the driver IC. In other words, the warpage of micro HDD affects the manufacturing process yield of driver IC. Mertol studies the low stress and low package warpage for the robust design of overmolded CSP on a flex_tape carrier with 280 solder balls for the second level interconnect with the package overall height less than 1.2 mm [7]. According to the practical experience in IC assembly, the warpage will result in a serious situation when the overall package height is less than 1.0 mm. This study focuses on the vertical dimension of driver IC in the specification of 0.65 mm and the warpage should be less than 100 μm after CSP assembly.

In this study, there are two chips in the driver IC: ASIC die is for logical control and memory die is responsible for read-and-write for buffer memory. There are 180 I/O leads in the CSP package, and the structure includes mold compound, silicon die, rigid substrate and copper trace materials, where the substrate is also serves as the connection between die and motherboard. The die is the signal generator and it controls all activity for the device. AND the CSP manufacturing processes of driver IC shows as Fig. 1. Based on practical experience, the important processes include thin molding, thin wafer, thin substrate process and molding compound materials, and there are three key material dimensions have to be controlled during the CSP process to meet the package overall height and low package warpage.

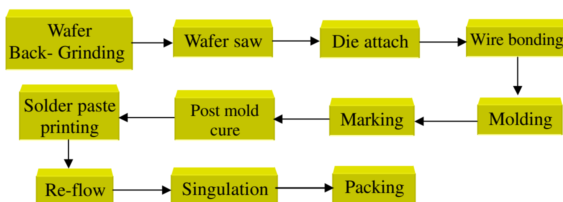

Fig. 1. The CSP manufacturing processes of driver IC.

In fact, the space in the micro HDD is quite limited. Since portable device are to be lighter, thinner, shorter and smaller, there is not much space for the IC package. Each package should be controlled in tight tolerance. Otherwise, it will be a micro HDD assembly issue. A vertical dimension (Z-axis) control of driver IC is crucial owing to the limited space in micro HDD. Fig. 2 illustrates the structure of the driver IC CSP packaging, where 'DS', 'GW', 'DT', 'DAT', 'MT' and 'ST' are die size, gold wire, die silicon thickness, die attachment material thickness, mold thickness, and substrate thickness, respectively. In addition, the mold thickness is one of the key materials and it is the major dimension to keep the overall package height ('MT' dimension in Fig. 2). The second key material dimension is die the thickness and it is a very importance process control item for the CSP assembly ('DT' dimension in Fig. 2). The third key material dimension is substrate thickness ('ST' dimension in Fig. 2).

The above materials (mold compound, silicon die, rigid substrate and copper trace) have different coefficients of thermal expansion (CTE). The major material characteristics are displayed in Table 1. Under cost constrains, this study uses a rigid substrate carrier. However, the rigid substrate is selected for this CSP, and the PCB warpage may change from 0% to 0.5%, which is less than the maximum warpage, 0.75%, for PCB board accepted by IPC [4]. On the molding, 0.5% warpage is achieved by a vertical displacement loading, which means the PCB at the most far corner board

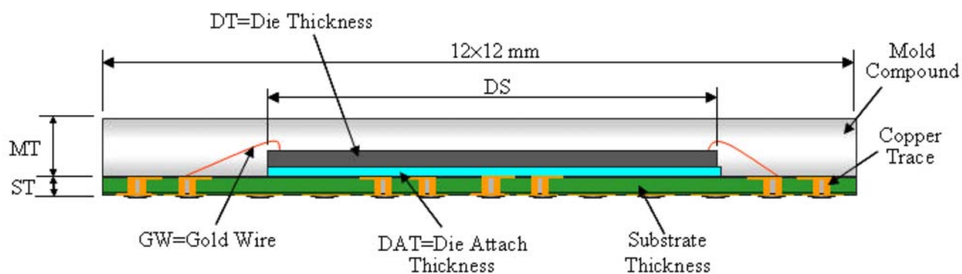

Fig. 2. Cross-sectional view of CSP package for micro HDD driver IC.

Table 1
The major material characteristics

Material items		Young's modulus (GPa)	CTE (ppm/°C)	T_g (°C)
Silicon		156.93	2.8	–
Copper		118.68	16.3	–
Die attach material		2.00	30/57	36
Mold compound		25.50	8/35	140
Substrate	Solder mask	3.50	60/140	105
	BT	24.04	14/14/58	–
	Copper	118.68	16.3	–

has a positive deformation upward in the vertical dimension. When the total height of the package is limited to $MT + ST \leqslant 0.65$ mm, selection of different combination of substrate thickness and mold thickness, the CTE miss match will occur during assembly thermal process, such as molding, post mold cure and re-flow process. In addition, the different combination will result in large variation of warpage level. In general, the mold thickness and substrate thickness are to define the package dimensions. Although the thinner mold thickness is preferred, the die thickness should be control to avoid gold wire exposure.

This study focuses on the vertical dimension of driver IC in the specification of 0.65 mm and the warpage should be less than 100 μm (smaller-the-better, STB) after CSP assembly. In this present study, the Taguchi method of parameter design using the static characteristic was employed for the robust design of CSP on a substrate carrier with less than 0.65 mm package height. So, the package warpage was defined as a key quality characteristic.

2. Experiments

Conventionally, engineers apply the Taguchi method to conduct parameter design in a variety of industrial practices. A Taguchi experiment consists of a set of experiments where the settings of the various design parameters that an engineer wants to study are changed from one experiment to another. The Taguchi experiments have been successfully applied on the optimum design of ball grid array packages [5,6]. Orthogonal arrays have been developed to accomplish experiment designs with a number of arrays. Orthogonal arrays are designated by the notation L (L for Latin squares) with a subscript. Mertol pointed out the significant control factors affecting package warpage are die thickness, die size, mold compound, substrate thickness, mold compound thickness and die attach thickness in the CSP package process [5,7]. Moreover, after molding process, the mold compound must be cured by curing oven, to get the stability of molding epoxy compound. In order to get the necessary characteristics of molding epoxy compound and production throughput, the cure temperature and cure time are studied in this experiment. In the study, the nine control factors included in Taguchi experiments are die thickness, die size, die attach thickness, mold thickness, mold compound, substrate thickness, cure temperature, cure time and package size. For each parameter, three levels are chosen to cover the range of interest. Twenty-seven trails are conducted by a well-structured orthogonal array L_{27}. The readers who are interested in Taguchi analysis should refer to [8]. Consequently, a $L_{27}(3^{13})$ orthogonal array design was used to find the optimum combination of parameter levels to attain lower package warpage. The control factors with chosen levels are listed in Table 2. In addition, to satisfy the lead-free materials requirement, based on the different *CTE* α *2* quality characteristics, different materials of mold compound were selected to observe the warpage change of the driver IC. Three mold compound experimental levels are displayed in Table 3.

The above control factors will influence the CTE performance on the CSP package. The warpage issue is the STB type and the required thickness is less than 100 μm (about 4 mils) after assembly process. This study aims to

Table 2
Control factors and their levels

Control factors	Variables	Levels		
		1	2	3
Die thickness (mm)	*A*	75 μm	100 μm	125 μm
Die size (mm)	*B*	6 × 6 mm	9 × 9 mm	12 × 12 mm
Die attach thickness (mm)	*C*	20 μm	30 μm	40 μm
Mold thickness (mm)	*D*	300 μm	350 μm	400 μm
Mold compound	*E*	M1	M2	M3
Substrate thickness (mm)	*F*	110 μm	130 μm	150 μm
Cure temperature (°C)	*G*	170	175	180
Cure time (h)	*H*	2 h	4 h	6 h
Package size (mm)	*I*	10 × 10 mm	12 × 12 mm	14 × 14 mm

Table 3
Mold compound material properties

	M1	M2	M3
CTE $\alpha 1$ (ppm/°C)	8	8	8
CTE $\alpha 2$ (ppm/°C)	25	30	35
T_g (°C)	140	140	140
Filler content (wt%)	89	89	89
Young modulus (GPa) @25 °C	25.5	25.5	25.5
Specific gravity	2.01	2.01	2.01
Curing temp. (°C)	175 ± 5	175 ± 5	175 ± 5
Curing time (h)	2–6	2–6	2–6

figure out the optimized conditions for the process response (warpage) by using Taguchi method. The signal-to-noise (S/N) ratio (η) is an index of robustness in experimental processing, and the definition of S/N ratio for the STB response is as follows:

$$\eta = \mathrm{SN_{STB}} = -10\log_{10}(\mathrm{MSD}),$$

where $\mathrm{MSD} = \frac{1}{n}\sum_{1}^{n} y_i^2$, y_i is the ith observation and n is the number of observation in each combination. According to the definition of S/N ratio in Taguchi method [8], the larger S/N ratio means the better product quality with less product loss, for example, −39 dB is better than −40 dB. The orthogonal array used in the study is $L_{27}(3^{13})$ with four repetitions for each combination. There are totally 108 observations in our study.

3. Results and discussion

The observations, means and S/N ratios for each experimental combination, are listed in Table 4. The highest S/N ratio is experiment 16th with $\eta = -38.0205$ dB and the average warpage = 78.945 μm.

The response table of S/N ratios for control factors is displayed in Table 5 and main effect plots for SN ratio shows as in Fig. 3. The ranks of the nine factors for a minimum warpage are D (mold thickness), E (mold compound), F (substrate thickness), I (package size), A (die thickness), B (die size), C (die attach thickness), G (cure temperature), and H (cure time).

The analysis of variance (ANOVA) in Table 6 shows the ranks of significance for control factors are D (mold thickness), E (mold compound), F (substrate thickness),

Table 4
Summary of experiment data

Experiment no.	Factors									Warpage	
	A	*B*	*C*	*D*	*E*	*F*	*G*	*H*	*I*	Average	S/N (dB)
1	1	1	1	1	1	1	1	1	1	95.504	−39.6031
2	1	1	1	1	2	2	2	2	2	97.062	−40.0154
3	1	1	1	1	3	3	3	3	3	127.935	−42.2508
4	1	2	2	2	1	1	1	2	2	88.138	−38.9822
5	1	2	2	2	2	2	2	3	3	87.820	−38.8970
6	1	2	2	2	3	3	3	1	1	96.480	−39.6946
7	1	3	3	3	1	1	1	3	3	104.765	−40.4239
8	1	3	3	3	2	2	2	1	1	111.760	−40.9959
9	1	3	3	3	3	3	3	2	2	129.365	−42.2897
10	2	1	2	3	1	2	3	1	2	104.140	−40.3799
11	2	1	2	3	2	3	1	2	3	110.744	−41.2926
12	2	1	2	3	3	1	2	3	1	94.615	−40.1646
13	2	2	3	1	1	2	3	2	3	96.520	−40.1477
14	2	2	3	1	2	3	1	3	1	106.680	−40.6657
15	2	2	3	1	3	1	2	1	2	108.070	−41.1828
16	2	3	1	2	1	2	3	3	1	83.005	−38.3892
17	2	3	1	2	2	3	1	1	2	99.903	−40.6728
18	2	3	1	2	3	1	2	2	3	111.506	−41.1682
19	3	1	3	2	1	3	2	1	3	84.327	−38.5958
20	*3*	*1*	*3*	*2*	*2*	*1*	*3*	*2*	*1*	*78.945*	*−38.0205*
21	3	1	3	2	3	2	1	3	2	90.395	−39.1645
22	3	2	1	3	1	3	2	2	1	101.285	−40.1116
23	3	2	1	3	2	1	3	3	2	98.164	−40.1037
24	3	2	1	3	3	2	1	1	3	110.346	−40.9754
25	3	3	2	1	1	3	2	3	2	107.696	−40.6653
26	3	3	2	1	2	1	3	1	3	100.874	−40.0880
27	3	3	2	1	3	2	1	2	1	92.425	−39.3314

Average $= \frac{1}{4}\sum_{i}^{4} y_i$.

Table 5
Response table for signal-to-noise ratios

Level	*A*	*B*	*C*	*D*	*E*	*F*	*G*	*H*	*I*
1	−40.350	−39.943	−40.366	−40.439	−39.700	−39.971	−40.124	−40.243	−39.664
2	−40.452	−40.085	−39.944	−39.287	−40.084	−39.811	−40.200	−40.151	−40.384
3	−39.673	−40.447	−40.165	−40.749	−40.691	−40.693	−40.152	−40.081	−40.427
Delta	0.779	0.504	0.422	1.461	0.992	0.883	0.076	0.163	0.763
Rank	4	6	7	1	2	3	9	8	5

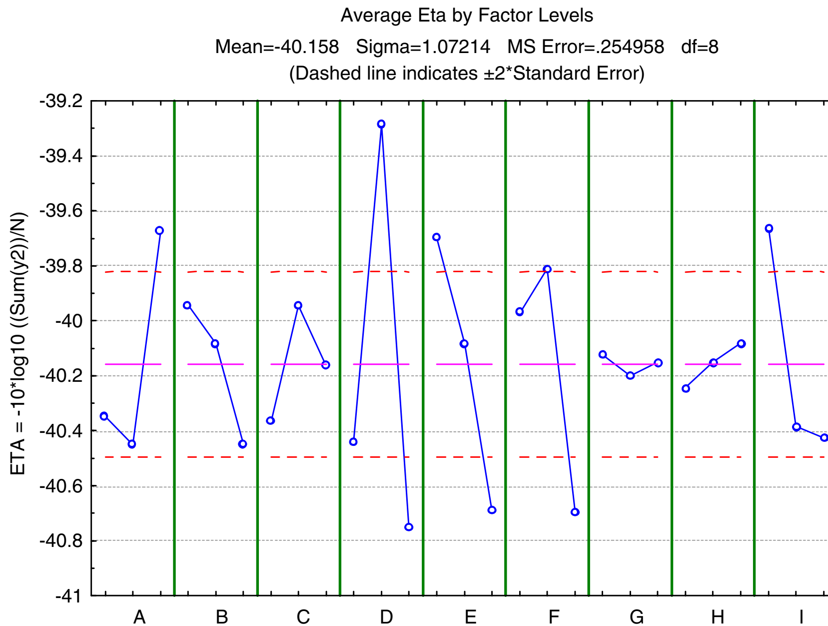

Fig. 3. Main effect plots for SN ratio.

Table 6
Analysis of variance using adjusted SS for tests

Source	SS	df	MS	*F*	*P*	Pure sum of square	Percent contribution (%)
A	3.226	2	1.6129	8.854	0.0043	2.861	9.53
B	1.217	2	0.6085	3.341	0.0703	0.853	2.84
C	0.801	2	0.4003	2.197	0.1538	0.436	1.45
D	10.674	2	5.3372	29.298	0.0000	10.310	34.33
E	4.500	2	2.2495	12.348	0.0012	4.135	13.77
F	3.979	2	1.9895	10.921	0.0020	3.615	12.04
G[a]	0.027	2	–	–	–	–	–
H[a]	0.120	2	–	–	–	–	–
I	3.305	2	1.6524	9.071	0.004	2.941	9.79
Residual	2.186	12	0.1822				16.26
Total	30.033						

[a] SS: sum of square, df: degree of freedom, MS: mean square, *F*: *F*-ratio, *P*: *P*-value.

I (package size), *A* (die thickness), *B* (die size), *C* (die attach thickness), *G* (cure temperature) and *H* (cure time). The low effects of factor *G* and *H* are combined with the error estimate to provide better estimate of

error variance. The percent contributions of warpage for micro HDD driver IC are 34.33%, 13.77%, 12.04%, 9.79%, and 9.53% for factors D, E, F, I and A. The percent contribution due to error is 16.26%. Thus, the factor levels can be determined as $A_3B_1C_2D_2E_1F_2G_1H_3I_1$ based on the above analysis.

The estimate of S/N ratio for $A_3B_1C_2D_2E_1F_2G_1H_3I_1$ is −37.0723 dB.

$$\hat{\eta} = \bar{T} + (\bar{A}_3 - \bar{T}) + (\bar{D}_2 - \bar{T}) + (\bar{E}_1 - \bar{T}) + (\bar{F}_2 - \bar{T}) + (\bar{I}_1 - \bar{T}) = -37.0723\ \text{dB}.$$

The purpose of the confirmation experiment is to validate the conclusions drawn during the analysis stage. The confidence intervals of the above estimation can be calculated as follows. Three confirmation experiments are carried out at the $A_3B_1C_2D_2E_1F_2G_1H_3I_1$ condition and the 95% confidence intervals for S/N ratio (CI_{STB}) are (-37.0723 ± 0.8039675), which are calculated as follows:

$$CI_{STB} = \sqrt{F_{\alpha;1;v2} \times V_e \times \left[\frac{1}{n_{eff}} + \frac{1}{r}\right]} = \sqrt{F_{0.05:1:10} \times 0.17533 \times \left[\frac{11}{27} + \frac{1}{3}\right]} = 0.8039675,$$

where $F_{\alpha;1;v2}$ is the F-ratio required for α risk, V_e the pooled error variance, r the number of the confirmation experiment and n_{eff} the effective sample size. The mean calculated from three S/N ratios for three confirmation experiments is equal to −36.956 dB, which is located within the confidence intervals. The result confirms the $A_3B_1C_2D_2E_1F_2G_1H_3I_1$ combinations of factor levels determined in the analysis phase.

Since large variability of CTE characteristic exists among different mold thickness and mold compound type or substrate thickness and mold thickness, the selection of proper combination of the above four materials is essential to control the warpage level. Besides, although it is true that the lower curing temperature results in the smaller warpage of the CSP package, the curing level is not fully completed when the curing temperature is too low, and this situation will cause the unstable operation of the driver IC. Thus, the curing temperatures in this study were set to (170, 175, 180). Finally, according to conclude the results from the above experiment, the optimal combination of the driver IC for micro HDD is $A_3B_1C_2D_2E_1F_2G_1H_3I_1$. That is, the die thickness should be thick, the die size should be 6×6 mm, the die attach thickness should be 30 μm, the mold thickness should be 350 μm, the mold compound should be level 'M1', the substrate thickness should be 130 μm, the cure temperature should be 170 °C, the cure time should be 6 h, and the package size should be 10 mm × 10 mm.

4. Conclusions

The size of driver IC for micro HDD becomes smaller and thinner, which enhances the difficulty of the follow-up manufacturing process. This study applies orthogonal array $L_{27}(3^{13})$ in Taguchi method to discover the combination of production levels of control factors to provide low production loss and reduce production variance. Results show that the $A_3B_1C_2D_2E_1F_2G_1H_3I_1$ combination can be viewed as reliable for the package overall height less than 0.65 mm of driver IC for micro HDD with CSP manufacturing process.

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