Interleaved Buck Converters with a Single-Capacitor Turn-Off Snubber

YAOW-MING CHEN, Member, IEEE
SHENG-YU TSENG
CHENG-TAO TSAI
TSAI-FU WU, Senior Member, IEEE
National Chung Cheng University
Taiwan

This paper proposes interleaved buck converters with a single-capacitor snubber to smooth out switch turn-off transition. The single-capacitor snubber is used to limit rising rate of drain-source voltage of the metal-oxide-semiconductor field-effect transistor (MOSFET) switch in the converters to reduce turn-off loss. In addition, the converters are operated at the boundary of continuous and discontinuous conduction modes (CCM), (DCM) to reduce turn-on loss, and in an interleaving fashion to reduce output current ripple. As compared with the counterparts of conventional converter topologies, the proposed converters have the merits of less component count, higher efficiency over a certain load range, smaller size, and they are easier to implement. Hardware measurements obtained from experimental prototypes have verified these merits.

Manuscript received May 30, 2003; revised May 18, 2004; released for publication June 10, 2004.

IEEE Log No. T-AES/40/3/835891.

Refereeing of this contribution was handled by W. M. Polivka.

Authros' address: Power Electronics Applied Research Laboratory (PEARL), Dept. of Electrical Engineering, National Chung Cheng University, Ming-Hsiung, Chia-Yi, 621 Taiwan, ROC, E-mail: (tfwu@ee.ccu.edu.tw).

I. INTRODUCTION

Buck converters are widely used as step-down dc/dc converters. To reduce size and weight of the converters, there is a trend to operate them at high switching frequencies. However, as the switching frequencies increase, switching loss, noise, and stress associated with turn-on and turn-off transitions also increase. These drawbacks reduce power conversion efficiency and powering capability, which in turn seriously deteriorate in system performance.

To alleviate the problems described above, several kinds of soft-switching converters, such as quasi-resonant converters (QRCs) [1–3], and multiresonant converters (MRCs) [4–6], have been used as step-down converters. In these converters, the switching devices are operated with either zero-voltage switching (ZVS) or zero-current switching (ZCS), reducing switching loss significantly. However, high voltage and current stress, large conduction loss, high load limitation, and high cost have restricted them from wide applications.

Most recent development in high frequency converters is those with a hybrid of resonant soft-switching feature and pulsewidth modulation (PWM) control, namely soft-switching PWM converters. They can relieve the drawbacks described previously. The converters are usually classified into two groups: passive soft-switching converters and active soft-switching converters. The passive ones use only passive components to achieve zero-current transition (ZCT) at turn on and zero-voltage transition (ZVT) at turn off [7–11]. The active ones incorporate passive components and auxiliary active switches to achieve soft-switching commutation [12–13], which would increase cost significantly at low or middle levels of power applications. Thus, a converter with passive soft-switching feature is more attractive to low power applications.

In a single passive soft-switching converter [11], as shown in Fig. 1, the buck converter is equipped with a lossless turn-off snubber to reduce turn-off loss and is operated at the boundary of discontinuous conduction mode (DCM) and continuous conduction mode (CCM) to reduce turn-on loss. Due to this operation, inductor current will swing over a wide range. To reduce ripple current and increase power level, two converters operated with an interleaving fashion, as shown in Fig. 2, are usually adopted [14–16], which also can achieve fast dynamic response and small ripple voltage. Although the two buck converters can achieve a soft-switching feature, their component count and cost are increased significantly. We propose soft-switching interleaved buck converters with a single-capacitor snubber, as shown in Fig. 3(b), to release the above discussed drawbacks. The converters require only a resonant capacitor C_1 which is associated with inductors L_1 and L_2 to function as a

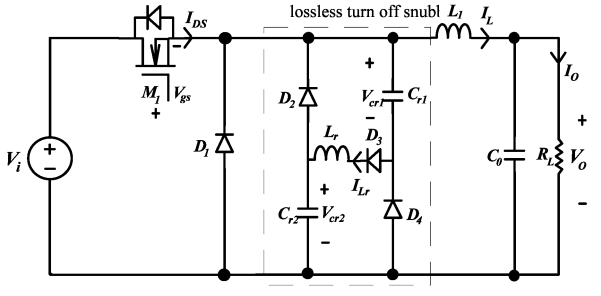


Fig. 1. Schematic diagram of buck converter with lossless turn-off snubber.

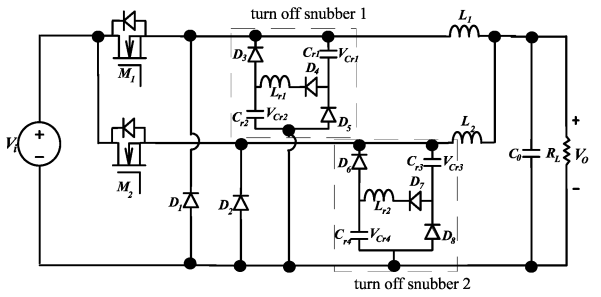


Fig. 2. Schematic diagram of interleaved buck converters with two turn-off snubbers.

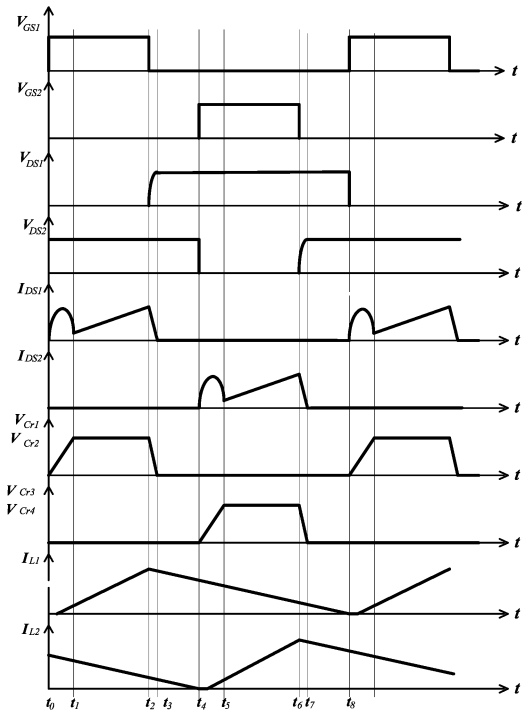


Fig. 4. Key waveforms of interleaved buck converters with two turn-off snubbers shown in Fig. 2.

lossless turn-off snubber, reducing switching loss and component count significantly. It should be pointed out that inductors L_1 and L_2 are loosely coupled to have correct operation in each buck converter.

II. DERIVATION OF PROPOSED CONVERTERS

To reduce switching loss, a lossless turn-off snubber is inserted in a conventional PWM power converter, as shown in Fig. 1. When switch M_1 is turned on, capacitors C_{r1} and C_{r2} are charged through inductor L_r and diode D_3 in a resonant manner. At the end of the resonant interval, capacitors C_{r1} and C_{r2} are charged up to V_i, and are clamped at V_i until switch M_1 is turned off. When switch M_1 is turned off, the charges stored in capacitors C_{r1} and C_{r2} are discharged to the output through diodes D_4 and D_2, respectively. Thus, switch M_1 is turned off with ZVT. As mentioned previously, although this converter can achieve high efficiency, its output current ripple is relatively large for high current and low output voltage applications. Therefore, to reduce output current ripple, an interleaving scheme is usually adopted. In the following, the proposed interleaved buck converter with a single-capacitor snubber is derived.

First, let us examine the conventional interleaved buck converters with two turn-off snubbers, as shown in Fig. 2. Their key waveforms are shown in Fig. 4 for operation reference. Essentially, these converters are composed of two single buck converters, as shown in Fig. 1, and their operations can be described straightforwardly. With the understanding of the converter operation, the converters shown in Fig. 2

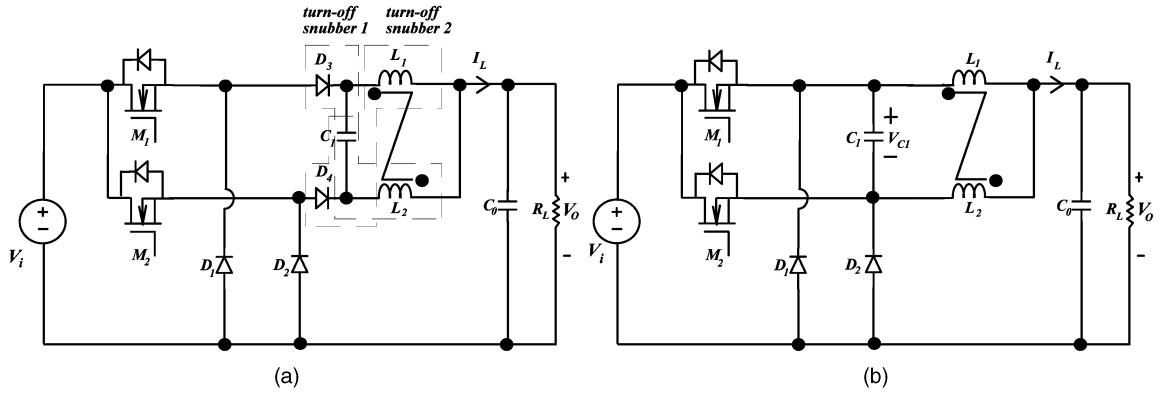


Fig. 3. Schematic diagram of proposed converters with single-capacitor snubber. (a) Intermediate stage. (b) Final stage.

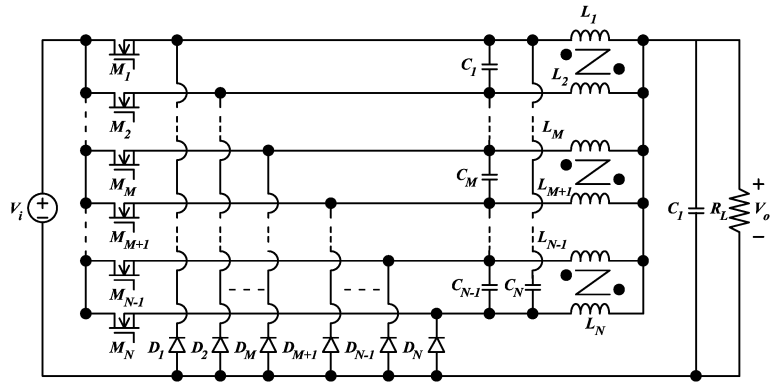


Fig. 5. Schematic diagram of interleaved N-buck converters with capacitor snubbers.

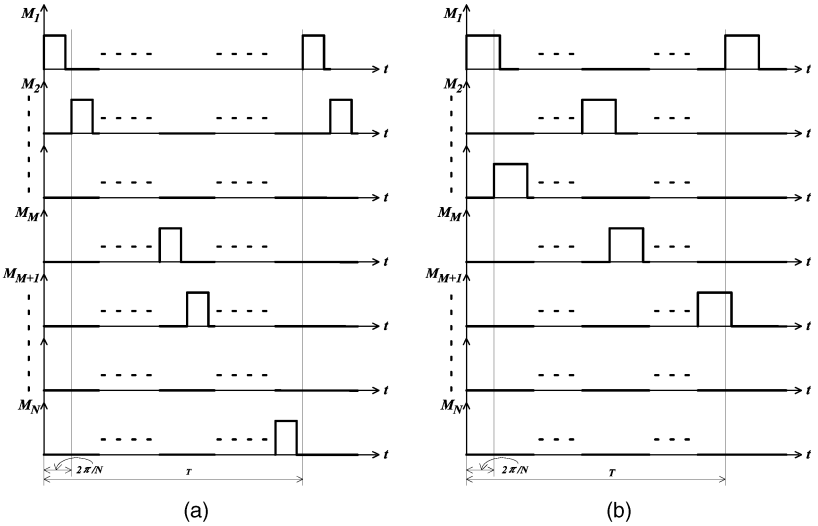


Fig. 6. Driving waveforms of interleaved N-buck converters with capacitor snubbers for (a) $D < 1/N$, and (b) $D \geq 1/N$.

can be degenerated as shown in Fig. 3(a). In the degeneration, inductors L_{r1} and L_{r2} shown in Fig. 2 are replaced with inductors L_1 and L_2 shown in Fig. 3(a), diodes D_3 and D_4 shown in Fig. 3(a) are used to replace D_4 and D_7 shown in Fig. 2, and capacitor C_1 in Fig. 3 is to replace $C_{r1} \sim C_{r4}$ in Fig. 2. In addition, diodes D_1 and D_2 shown in Fig. 3 will serve for discharging capacitor C_1, and they function the same as the diodes D_3, D_5, D_6, and D_8 shown in Fig. 2. According to the operation of the converters shown in Fig. 3(a), since diodes D_3 and D_4 are always in forward bias or zero bias, they can be removed (i.e., shorted). Thus, the converters can be degenerated into the ones shown in Fig. 3(b).

In high power-level applications, power converters need multiphase to supply power to loads. The multiphase buck converters, as shown in Fig. 5, can be formed from $N/2$ sets of the proposed interleaved buck converters, where N is limited to be an even number for simple discussion. Operation of the N-buck converters is subjected to the constrain that the switches of the Mth and $(M + 1)$th buck converters cannot turn on simultaneously and the duty ratio D of each converter cannot be greater than 0.5. In operation of the N buck converters, their duty ratios can have two choices, $D < 1/N$ and $D \geq 1/N$. When $D < 1/N$, sequential driving waveforms, as shown in Fig. 6(a), can be adopted to drive the N-buck converters, which can prevent the switches in the adjacent converters from turning on simultaneously. When $D \geq 1/N$, the sequence of driving waveforms cannot be continuous, as shown in Fig. 6(b).

III. OPERATION OF PROPOSED CONVERTER

The proposed converters, as shown in Fig. 3(b), consist of two buck converters and a single-capacitor snubber. These two converters are operated in an interleaving fashion to reduce output voltage ripple, at the boundary of CCM and DCM to reduce turn-on loss, and with a single-capacitor snubber to smooth out switch turn-off transition. The snubber consists of capacitor C_1 and either inductor L_1 or L_2. When either switch M_1 or M_2 is turned on, capacitor C_1 is charged up to V_i through coupled inductor L_1 or L_2. While, at the switch turn-off transition, capacitor C_1 will help to supply part of load power, achieving a ZVT feature. The coupled inductors serve not only as

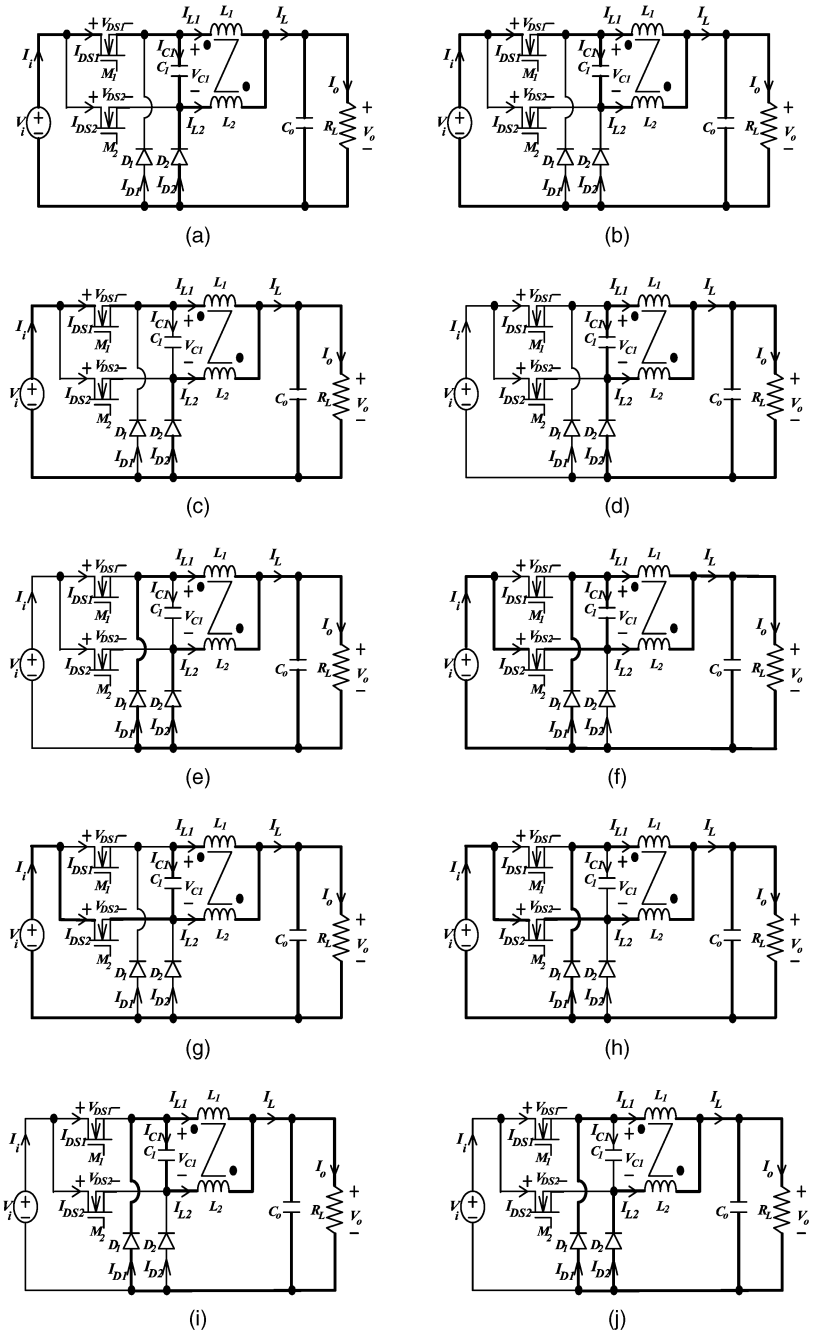


Fig. 7. Operational modes of proposed converters over one switching cycle. (a) Mode 1 ($t_0 - t_1$). (b) Mode 2 ($t_1 - t_2$). (c) Mode 3 ($t_2 - t_3$). (d) Mode 4 ($t_3 - t_4$). (e) Mode 5 ($t_4 - t_5$). (f) Mode 6 ($t_5 - t_6$). (g) Mode 7 ($t_6 - t_7$). (h) Mode 8 ($t_7 - t_8$). (i) Mode 9 ($t_8 - t_9$). (j) Mode 10 ($t_9 - t_{10}$).

the bulk inductors of the power stages but also as the snubber inductors.

Operation of the overall converters is divided into ten modes, as illustrated in Fig. 7, and their key waveforms are illustrated in Fig. 8. In the following, each operational mode is described briefly.

Mode 1 [Fig. 7(a), $t_0 \le t < t_1$]: Before t_0, diode D_2 is in freewheeling, and inductor current I_{L2} is equal to diode current I_{D2}. At $t = t_0$, switch M_1 is turned on. The equivalent circuit at this interval is shown in Fig. 7(a), from which it can be found that inductor current I_{L2} is equal to the sum of diode current I_{D2} and capacitor current I_{C1}. Since the interval of $t_0 \sim t_1$ is very short, inductor current I_{L1} is approximately equal to 0 A and capacitor voltage V_{C1} is close to 0 V. Thus, switch current I_{DS1} is approximately equal to capacitor current I_{C1}. During this interval, the current I_{C1} is abruptly increased up to inductor current I_{L2} and I_{D2} is abruptly decreased down to 0 A.

Mode 2 [Fig. 7(b), $t_1 \le t < t_2$]: At time t_1, capacitor current I_{C1} is equal to inductor current I_{L2},

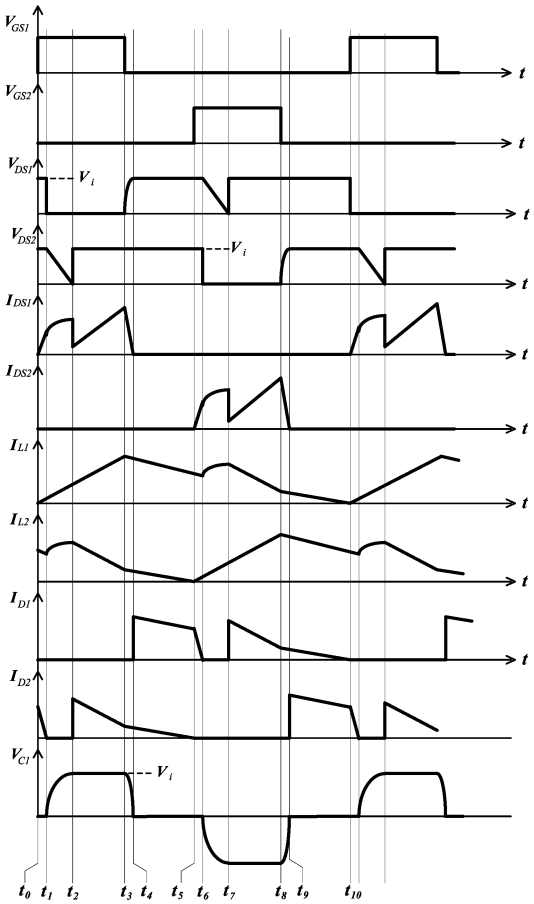


Fig. 8. Key waveforms of proposed converters operating over switching period.

and diode D_2 is reversely biased. At this time interval, snubber capacitor C_1 resonates with inductor L_2, and the switch current I_{DS1} is just equal to the sum of resonant inductor current I_{L2} $(= I_{C1})$ and inductor current I_{L1}. This time interval can be determined as follows:

$$t_{g1} = t_2 - t_1 = [\cos^{-1}(-V_0/(V_i - V_0))]\sqrt{L_1C_1} = [\cos^{-1}(-V_0/(V_i - V_0))]\sqrt{L_2C_1} \quad (1)$$

where t_{g1} denotes a time interval between t_1 and t_2, V_i is input voltage and V_o is output voltage. If V_i is far greater than V_o, (1) can be rewritten as follows:

$$t_{g1} = t_2 - t_1 = \frac{\pi}{2}\sqrt{L_1C_1} = \frac{\pi}{2}\sqrt{L_2C_1}. \quad (2)$$

At the same time, capacitor current I_{C1} reaches its maximum value which can be expressed as follows:

$$I_{C1} = \frac{V_i - V_o}{Z_O} \quad (3)$$

where Z_O is the characteristic impedance of $L_1 - C_1$ or $L_2 - C_1$ network, which is equal to $\sqrt{L_1/C_1}$ or $\sqrt{L_2/C_1}$.

Mode 3 [Fig. 7(c), $t_2 \le t < t_3$]: When $t = t_2$, capacitor voltage V_{C1} is equal to V_i and diode D_2 starts freewheeling through inductor L_2 while switch M_1 is still in the on state. The switch current I_{DS1} is now equal to inductor current I_{L1} which increases linearly, while inductor current I_{L2} is decreased linearly.

Mode 4 [Fig. 7(d), $t_3 \le t < t_4$]: At time t_3, switch M_1 is turned off. Because inductor current I_{L1} must be continuous, capacitor C_1 starts to discharge for holding a continuous inductor current. Thus, switch M_1 can be turned off with ZVT.

Mode 5 [Fig. 7(e), $t_4 \le t < t_5$]: When time reaches t_4, the voltage V_{C1} across capacitor C_1 is discharged toward zero and diode D_1 starts freewheeling. During this time interval, diodes D_1 and D_2 are in freewheeling through inductors L_1 and L_2, respectively.

Mode 6 [Fig. 7(f), $t_5 \le t < t_6$]: At time t_5, diode D_1 is still in freewheeling, but diode D_2 stops freewheeling because inductor current I_{L2} drops to zero. At the same moment, switch M_2 is turned on. Inductor current I_{L1} is equal to the sum of diode current I_{D1} and capacitor current $-I_{C1}$. Additionally, because the switch current I_{DS2} will flow through the low-impedance path of capacitor C_1, diode current I_{D2} will be dominated by the switch current I_{DS2}. That is, within this duration, capacitor current $-I_{C1}$ is approximately equal to the switch current I_{DS2}. During this interval, capacitor current $-I_{C1}$ is abruptly increased up to inductor current I_{L1} and I_{D1} is abruptly decreased down to 0 A.

Mode 7 [Fig. 7(g), $t_6 \le t < t_7$]: At time t_6, diode D_1 is reversely biased and resonant network formed by capacitor C_1 and inductor L_1 starts resonating. The switch current I_{DS2} is equal to the sum of inductor current I_{L1} $(= -I_{C1})$ and inductor current I_{L2}, and capacitor C_1 is reversely charged.

Mode 8 [Fig. 7(h), $t_7 \le t < t_8$]: At $t = t_7$, the capacitor voltage V_{C1} goes down to $-V_i$. The time interval lasts approximately a quarter of the resonant cycle as determined in (2). At the same moment, capacitor current $-I_{C1}$ reaches its maximum value, which can be expressed by (3). During this mode, diode D_1 starts freewheeling and inductor current I_{L2} is increased linearly.

Mode 9 [Fig. 7(i), $t_8 \le t < t_9$]: At time t_8, switch M_2 is turned off. Since the inductor current I_{L2} must be in smooth transition, capacitor voltage will drop to maintain a continuous inductor current. When $t = t_9$, capacitor voltage V_{C1} drops to zero.

Mode 10 [Fig. 7(j), $t_9 \le t < t_{10}$]: During this time interval, diodes D_1 and D_2 are in freewheeling through inductors L_1 and L_2, and their currents I_{D1} and I_{D2} are decreased linearly. When switch M_1 is turned on again at the end of mode 10, a new switching cycle will start.

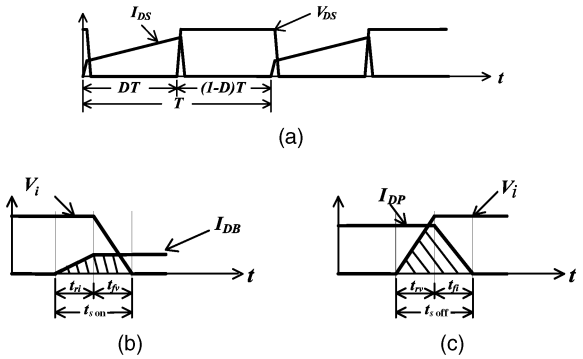


Fig. 9. Conceptual current and voltage waveforms of active switch. (a) Over one switching cycle. (b) During turn-on transition. (c) During turn-off transition.

IV. ANALYSIS OF SWITCHING AND CONDUCTION LOSS

Switching power converters using lossless turn-off snubbers to achieve soft-switching features usually need inductors or capacitors. The devices can help to reduce switching loss, while they induce extra conduction loss. To objectively evaluate the effectiveness of a lossless turn-off snubber, switching and conduction losses in a buck converter with the snubber are analyzed.

A. Switching Loss

In a buck converter, switching loss includes switch turn-on loss and switch turn-off loss, as illustrated in Fig. 9. At turn-on transition, two time intervals t_{ri} and t_{fv} are mainly involved, as shown in Fig. 9(b), and the switching loss can be approximated as

$$W_{s\,\mathrm{on}} = \frac{t_{s\,\mathrm{on}}}{2} V_i I_{DB}, \tag{4}$$

where $t_{s\,\mathrm{on}} = t_{ri} + t_{fv}$, V_i is the voltage across the switch and I_{DB} is its current. During turn-off transition, another two time intervals, t_{rv} and t_{fi}, are involved, as shown in Fig. 9(c). The turn-off loss therefore can be approximated as

$$W_{s\,\mathrm{off}} = \frac{t_{s\,\mathrm{off}}}{2} V_i I_{DP} \tag{5}$$

where $t_{s\,\mathrm{off}} = t_{rv} + t_{ri}$. From (3) and (4), the total switching losses over a switching cycle can be determined as follows:

$$W_{s\,\mathrm{total}} = W_{s\,\mathrm{on}} + W_{s\,\mathrm{off}} = \tfrac{1}{2} V_i (t_{s\,\mathrm{on}} I_{DB} + t_{s\,\mathrm{off}} I_{DP}). \tag{6}$$

B. Conduction Loss

When the buck converter is operated at CCM, the switch current waveforms appear like the ones shown in Fig. 10. According to the figure, conduction loss over a switching period can be determined as

$$W_{CC} = \tfrac{1}{3} t_{\mathrm{on}} R_{ds} (I_{DB}^2 + I_{DB} I_{DP} + I_{DP}^2), \tag{7}$$

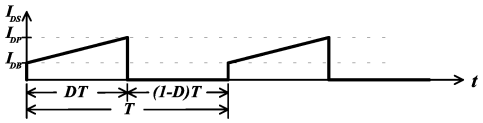


Fig. 10. Conceptual current waveforms of active switch in buck converter operated in CCM.

where $t_{\mathrm{on}} = DT$ is the conduction time, I_{DB} is the initial current, I_{DP} is the peak current, and R_{ds} is an equivalent conduction resistance of the switch. Therefore, if the buck converter is operated at the boundary of CCM and DCM, I_{DB} is equal to zero and the conduction loss can be expressed as follows:

$$W_{CD} = \tfrac{1}{3} t_{\mathrm{on}} R_{ds} I_{DP}^2. \tag{8}$$

C. Extra Conduction Loss due to Turn-off Snubber

To reduce switching loss, a buck converter is equipped with a turn-off snubber, as shown in Fig. 1. When switch M_1 is turned on, capacitors C_{r1} and C_{r2} are charged up to V_i, which will induce extra conduction loss to the active switch, as illustrated in Fig. 11(a). From Fig. 11(a), the instantaneous power loss can be determined as

$$P_{ES1} = \frac{R_{ds} C V_i^2}{2L_r} (1 - \cos 2\omega_{r1} t) \tag{9}$$

where ω_{r1} is the resonant frequency which is equal to $1/\sqrt{L_r C_{r1}}$ or $1/\sqrt{L_r C_{r2}}$ and $C = C_{r1}/2 = C_{r2}/2$. Thus, integration of P_{ES1} can yield the energy loss W_{ES1} which can be determined as

$$W_{ES1} = \int_0^{t_{p1}} P_{ES1}\, dt = \frac{\pi}{2\sqrt{L_r/C}} R_{ds} C V_i^2 \tag{10}$$

where $t_{p1} = \pi\sqrt{L_r C_{ri}} = \pi\sqrt{L_r C_{r2}}$.

If the buck converter is with a single-capacitor snubber, as shown in Fig. 3(b), to achieve a soft-switching feature, the conduction time interval of the resonant circuit which consists of capacitor C_1 and inductor L_1 or L_2 lasts only a quarter of the resonant cycle. The extra conduction loss can be approximately expressed as

$$W_{ES2} = \int_0^{t_{g1}} P_{ES2} = \frac{\pi(1-D)^2}{4\sqrt{L_1/C_1}} R_{ds} C_1 V_i^2 \tag{11}$$

where L_1 is the output inductor which is equal to L_2, and P_{ES2} can be determined form Fig. 9(b) as

$$P_{ES2} = \frac{R_{ds} C_1 (1-D)^2 V_i^2}{2L_1} (1 - \cos 2\omega_{r2} t), \tag{12}$$

where ω_{r2} is the resonant frequency which is equal to $1/\sqrt{L_1 C_1}$ or $1/\sqrt{L_2 C_1}$.

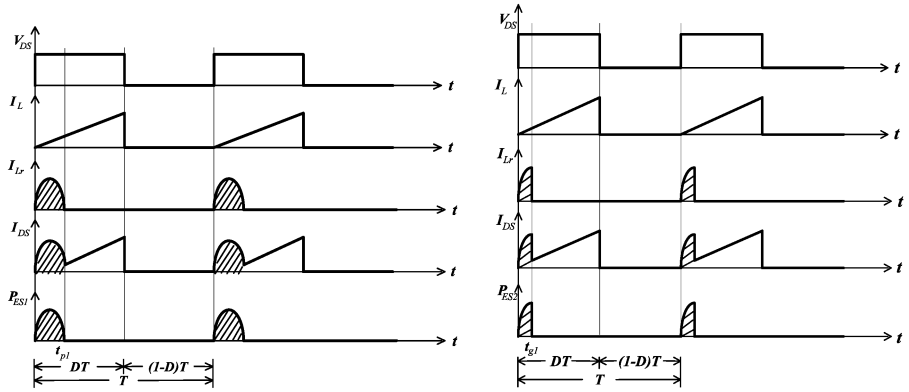


Fig. 11. Ideal current and voltage waveforms for illustrating extra conduction loss. (a) Buck converters with two turn-off snubbers. (b) Proposed ones with single-capacitor snubber.

V. DESIGN CONSIDERATIONS

To realize the proposed soft-switching converters systematically, design considerations of the coupled inductors L_1 and L_2 sharing an EI core, and the snubber capacitor C_1 are presented as follows. Additionally, limitation on duty ratio of the converters is also addressed in this section.

A. Design of Coupled Inductors

To reduce the size of the proposed converters, the two coupled inductors are designed with an EI core, as shown in Fig. 12. Their coupling relationship can be described as follows:

$$v_1 = L_1 \frac{di_{L1}}{dt} + M \frac{di_{L2}}{dt} \tag{13}$$

and

$$v_2 = M \frac{di_{L1}}{dt} + L_2 \frac{di_{L2}}{dt} \tag{14}$$

where v_1 and v_2 are the voltages applied on the two corresponding windings. In the above equations, mutual inductance M can be positive or negative, depending on coupling directions. Its equivalent circuits for each coupling direction are shown in Fig. 13, in which the ones shown in Fig. 13(a) will result in a positive M, while those shown in Fig. 13(b) will yield a negative M. Because inductors with inversely coupling method will yield better steady state and dynamic performance [14], it is adopted in the system to raise efficiency.

According to the operating principle of the buck converter, the voltage across the coupled inductor can be either $(V_i - V_o)$ or $-V_o$. During the switch turn-on interval, the voltage is $(V_i - V_o)$, while at the turn-off interval the voltage is $-V_o$. To simplify design process, the coupled inductors are designed with a symmetric structure, i.e. $L_1 = L_2 = L$. As a result, (12) and (13)

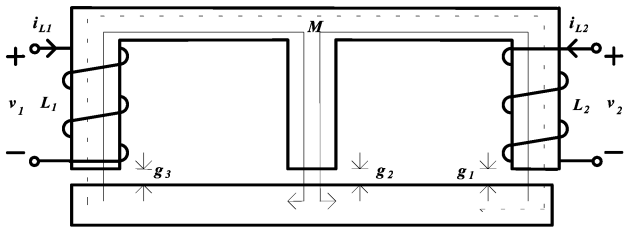


Fig. 12. Core structure of two coupled inductors used in proposed converters.

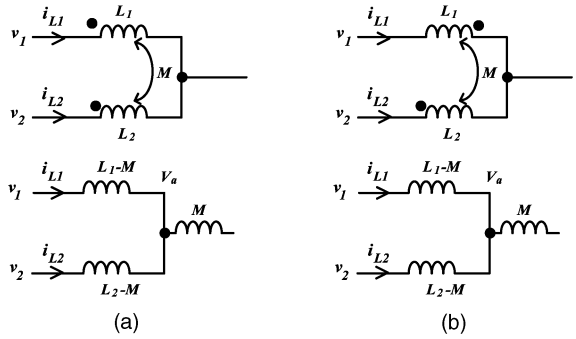


Fig. 13. Illustration of coupling directions of two coupled inductors.

can be rewritten as follows:

$$(v_1 - kv_2) = (1 - k^2)L \frac{di_{L1}}{dt} \tag{15}$$

where $k = M/L$. If the relationship between v_1 and v_2 can be found, (14) can be rewritten as

$$v_1 = \left(L_{\text{eq}} \frac{di_{L1}}{dt} \right) / (1 - kg_v) \tag{16}$$

where L_{eq} is an equivalent inductor which is equal to $(1 - k^2)L$ and $g_v = v_2/v_1$. When the relationship between v_1 and v_2 changes with time over a switching cycle, the parameter g_v in (15) will vary correspondingly.

In the proposed interleaved buck converters, the duty ratio is limited to be less than 0.5, and its

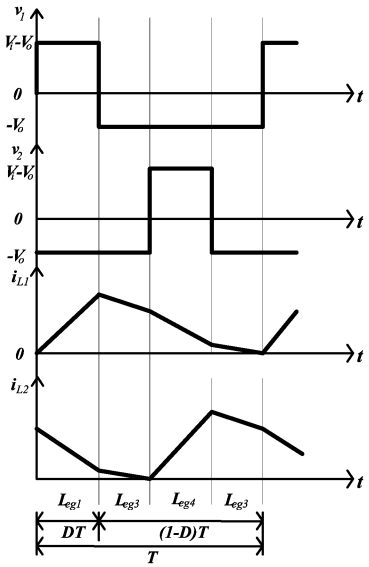


Fig. 14. Steady-state voltage and current waveforms of coupled inductors with conditions of $M < 0$ and $D \leq 0.5$.

corresponding key waveforms are shown in Fig. 14. Ideal operation of the converters can be divided into four time intervals over a switching cycle. Thus, according to volt-second balance theorem, there are four possible relationships between v_1 and v_2 which can be used to determine g_v, and they are expressed as follows:

1) when $v_1 = v_x$ and $v_2 = v_y$, $v_2 = -(D/D')v_1$ and $g_{v1} = -(D/D')$ (17)

2) when $v_1 = v_x$ and $v_2 = v_x$, $v_2 = v_1$ and $g_{v2} = 1$ (18)

3) when $v_1 = v_y$ and $v_2 = v_y$, $v_2 = v_1$ and $g_{v3} = 1$ (19)

4) when $v_1 = v_y$ and $v_2 = v_x$, $v_2 = -(D'/D)v_1$ and $g_{v4} = -(D'/D)$ (20)

where $v_x = v_i - v_o$, $v_y = -v_o$ and $D' = 1 - D$. From the above relationships, four corresponding equivalent inductances can be determined as

1) $L_{\text{eq1}} = L_{\text{eq}}/(1 - kg_{v1}) = (1 - k^2)L/(1 + Dk/D')$ (21)

2) $L_{\text{eq2}} = L_{\text{eq}}/(1 - kg_{v2}) = (1 + k)L$ (22)

3) $L_{\text{eq3}} = L_{\text{eq}}/(1 - kg_{v3}) = (1 + k)L$ (23)

4) $L_{\text{eq4}} = L_{\text{eq}}/(1 - kg_{v4}) = (1 - k^2)L/(1 + D'k/D)$. (24)

With these equivalent inductances, the proposed converters can be designed to operate at the boundary of CCM and DCM, and achieve higher efficiency. In terms of the four equivalent inductances, equivalent inductance $L_{T\text{eq}}$ of a noncoupled inductor can be determined as

$$L_{T\text{eq}} = \frac{L_{\text{eq1}}L_{\text{eq3}}}{(1-D)(1-2D)L_{\text{eq1}} + 2D(1-D)L_{\text{eq3}}}. \tag{25}$$

B. Design of Snubber Capacitor

In the proposed converters, capacitor C_1 resonates with inductors L_1 or L_2 to smooth out switch turn-off transition. The energy stored in C_1 can be determined as

$$W_{c1} = \tfrac{1}{2}C_1V_i^2. \tag{26}$$

To completely eliminate the switch turn-off loss, the energy stored in capacitor C_1 must be at least equal to the turn-off loss $W_{s\text{off}}$, as shown in (4), on which capacitance of C_1 can be determined as

$$C_i \geq \frac{I_{DP}}{V_i}t_{s\text{off}}. \tag{27}$$

The peak current I_{C1} of capacitor C_1 should be limited to being less than the peak values of I_{DS1} and I_{DS2}, so it will not increase the current ratings of switches M_1 and M_2. To eliminate turn-off loss $W_{s\text{off}}$ completely at different operation conditions, the time $t_{s\text{off}}$ is approximately equal to 500 ns in practical design considerations.

C. Limitation on Duty Ratio

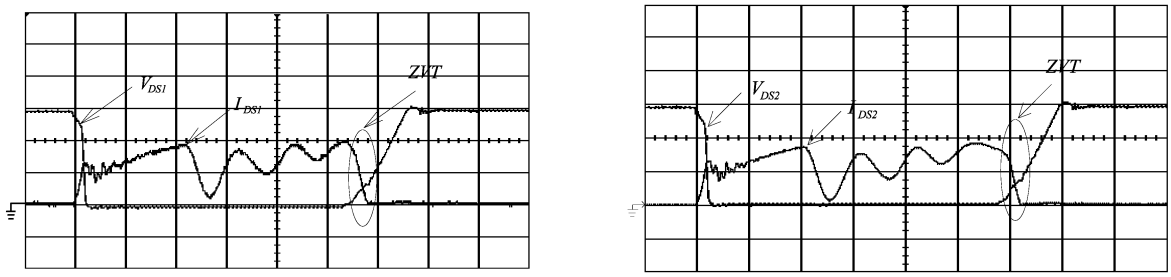
The proposed converters introduce a single-capacitor snubber to smooth out switch turn-off transition, which will induce turn-on loss to the proposed converters. A proper selection of capacitor C_1 can yield higher efficiency. Once the component value of capacitor C_1 has been determined, duty ratios of the proposed converters are also limited to a certain range, so as the sum of extra conduction loss W_{ES2} and turn-on loss $W_{S\text{on}}$ is always less than the turn-off loss $W_{s\text{off}}$. A limitation on the duty ratio can be expressed as

$$\frac{\left(1-\frac{t_{s\text{on}}}{2t_{s\text{off}}}\right) - \sqrt{\left(1-\frac{t_{s\text{on}}}{2t_{s\text{off}}}\right)^2 - \frac{2\pi R_{ds}C_1L_1}{T_st_{s\text{off}}\sqrt{L_1/C_1}}}}{2} \leq D \leq \frac{\left(1-\frac{t_{s\text{on}}}{2t_{s\text{off}}}\right) + \sqrt{\left(1-\frac{t_{s\text{on}}}{2t_{s\text{off}}}\right)^2 - \frac{2\pi R_{ds}C_1L_1}{T_st_{s\text{off}}\sqrt{L_1/C_1}}}}{2} \tag{28}$$

where T_S is the switching period.

VI. Measurement and Discussion

To verify the analysis and discussion, a Peltier-device application (for air conditioning) with



(50V/div, 5A/div, 0.5us/div) (a)

(50V/div, 5A/div, 0.5us/div) (b)

Fig. 15. Measured voltage and current waveforms of switches in proposed converters. (a) Switch M_1. (b) Switch M_2.

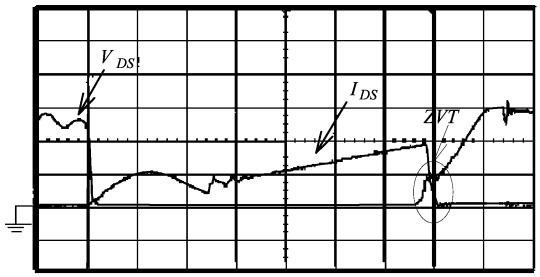
the following specifications is implemented

input voltage: 156 Vdc
output voltage: 24 Vdc
output current: 10 A
switching frequency: 50 kHz
maximum output power: $P_{\max} = 240$ W.

From (27), value of snubber capacitor C_1 can be calculated as 32 nF. In our design example, a capacitor with 33 nF is adopted. In inductor design, the coupling coefficient K of the loosely coupled inductors L_1 and L_2 is chosen as 0.33. According to the operational principle of a buck converter and from (21)–(25), inductor L_{Teq} is determined to be 40 μH and $L_1 = L_2 = 30$ μH. In summary, the components of the buck converter power stage are determined as follows:

M_1, M_2: IRFP 250
D_1, D_2: MUR1560
C_0: 470 μF
L_1, L_2: 30 μH
C_1: 33 nF
inductor core: EE-35.

The measured voltage and current waveforms of the switches with the proposed single-capacitor snubber and with two turn-off snubbers are shown in Fig. 15 and Fig. 16, respectively. From Figs. 15 and 16, although we can observe that each power switch is turned off with ZVT, there still exists significant difference. In Fig. 15, the drain-source voltage transition at turn off is smooth because before switch M_1 or M_2 is turned off, capacitor voltage V_{C1} is always clamped to V_i. That is, at switch M_1 or M_2 turn-off transition, the drain-source voltage will start to rise from 0 V. However, in Fig. 16, due to nonideal characteristics of snubber components, such as parasitic resistor, inductor and capacitor, voltages V_{Cr1}, V_{Cr2}, V_{Cr3}, and V_{Cr4} of the snubber capacitors cannot be charged up to V_i. Thus, the capacitors cannot supply energy until diode D_1 or D_2 is in forward bias, causing an abrupt change at turn-off transition and resulting in more switching loss. It should be noted that current ringing has been observed in Fig. 15. This ringing is primarily due to the parasitic capacitor



(50V/div, 5A/div, 0.5us/div)

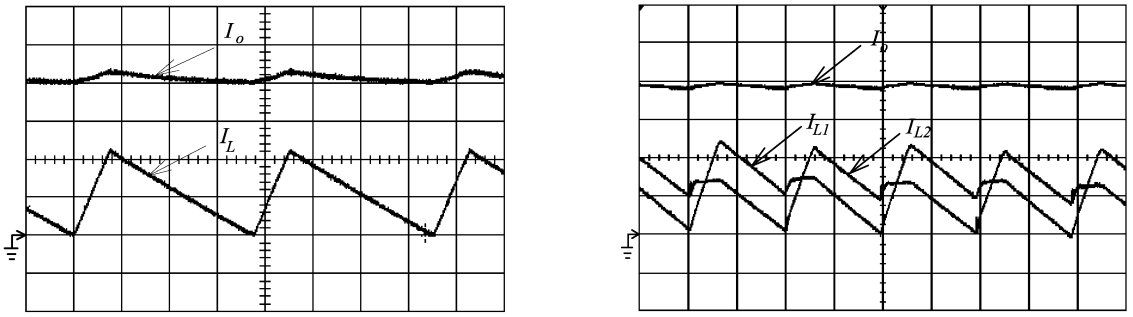
Fig. 16. Measured voltage and current waveforms of switches in interleaved buck converters with two turn-off snubbers.

of diode D_1 or D_2 and coupled inductor L_1 or L_2 in resonating after capacitor V_{C1} reaches V_i.

For comparison, the measured waveforms of inductor current I_L and output current I_o of a single buck converter with a lossless snubber, as shown in Fig. 1, are shown in Fig. 17(a), while the ones of the proposed interleaved converters are shown in Fig. 17(b). It reveals that the proposed converter can reduce the ripple of the output current I_o.

To make a fair comparison, the hardware components of the proposed converters, hard-switching buck converters, and those with two turn-off snubbers are kept as the same as possible. Fig. 18 shows the plots of output voltage and current waveforms of the three kinds of converters under step-load changes between 20% and 100% with a repeat rate of 1 kHz and a duty ratio of 50%. From Fig. 18, it can be observed that although the proposed converters are using less number of component counts, they yield almost the same dynamic performance as those with complicated configurations.

Comparisons among the efficiencies of the proposed converters and their counterparts are illustrated in Fig. 19. It can be observed that the proposed converters cannot always yield higher efficiencies than the others under various operating conditions. It has a trend that at lower output-voltage levels, the proposed converters and the ones with two



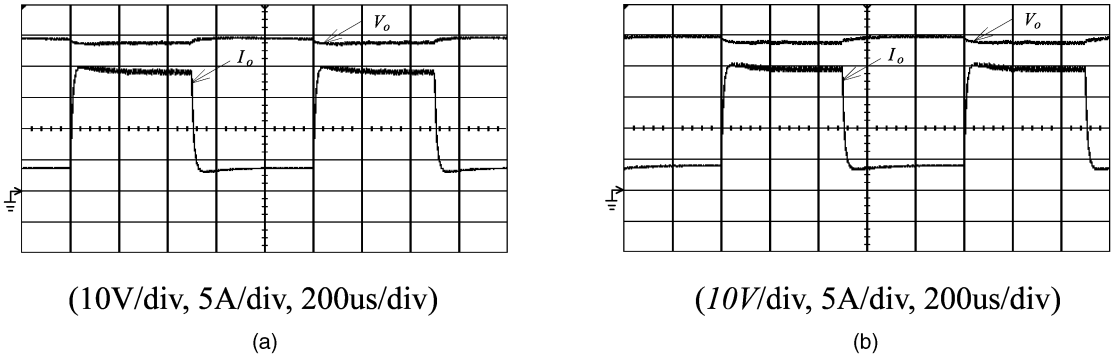
(I_o: 2.5A/div, I_L: 5A/div, 5us/div)

(a)

(I_o: 2.5A/div, I_{L1}, I_{L2}: 5A/div, 5us/div)

(b)

Fig. 17. Measured waveforms of inductor current I_L and output current I_O of (a) single buck converter, and (b) proposed interleaved buck converters.

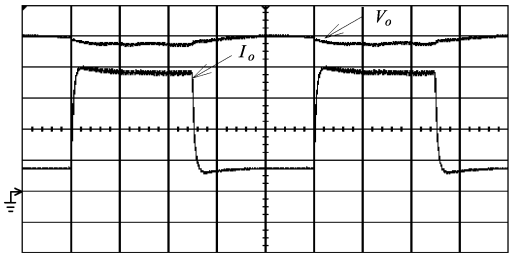


(10V/div, 5A/div, 200us/div)

(a)

(*10V*/div, 5A/div, 200us/div)

(b)



(*10V*/div, 5A/div, 200us/div)

(c)

Fig. 18. Output voltage V_o and output current I_o under step-load changes between 20% and 100% of full load of discussed interleaved buck converters with (a) hard switching, (b) two turn-off snubbers, and (c) proposed single-capacitor snubber.

turn-off snubbers can yield higher efficiency, while at higher ones, all of these three types of converters yield almost the same efficiency. The reasons behind are that given a fixed power level, a lower output voltage level will result in higher switch currents and the turn-off loss $W_{s\text{off}}$ will be much higher than the sum of the extra conduction loss W_{ES2} and switching loss $W_{s\text{on}}$. According to (28) and the component values listed in Table I, the range of duty ratio D can be determined to yield higher efficiency than that of a hard-switching one and its range varies theoretically from 0.011 to 0.239. On the other hand, when output voltage V_o is greater than 37 V (i.e., $D >$ 0.239), efficiency of the hard-switching converters is greater than that of the proposed converters with a single-capacitor snubber. Comparisons of performance and power loss among the discussed converters are collected in Table II and Table III, respectively.

In the proposed converters, although they are operated at the boundary of CCM and DCM, there still exists switching loss at switches M_1 and M_2 turn-on transition, as illustrated in Fig. 15. This loss is due to the snubber capacitor C_1. In the proposed operational principle, when both switches M_1 and M_2 are in the off states and if inductor current I_{L1} has dropped to zero, inductor current I_{L2} will not run dry yet. Next, when switch M_1 is turned on while switch M_2 is kept in the off state, diode D_1 will be reversely biased and diode D_2 will be in forward conduction. Since a high inrush switch current I_{DS1} will flow

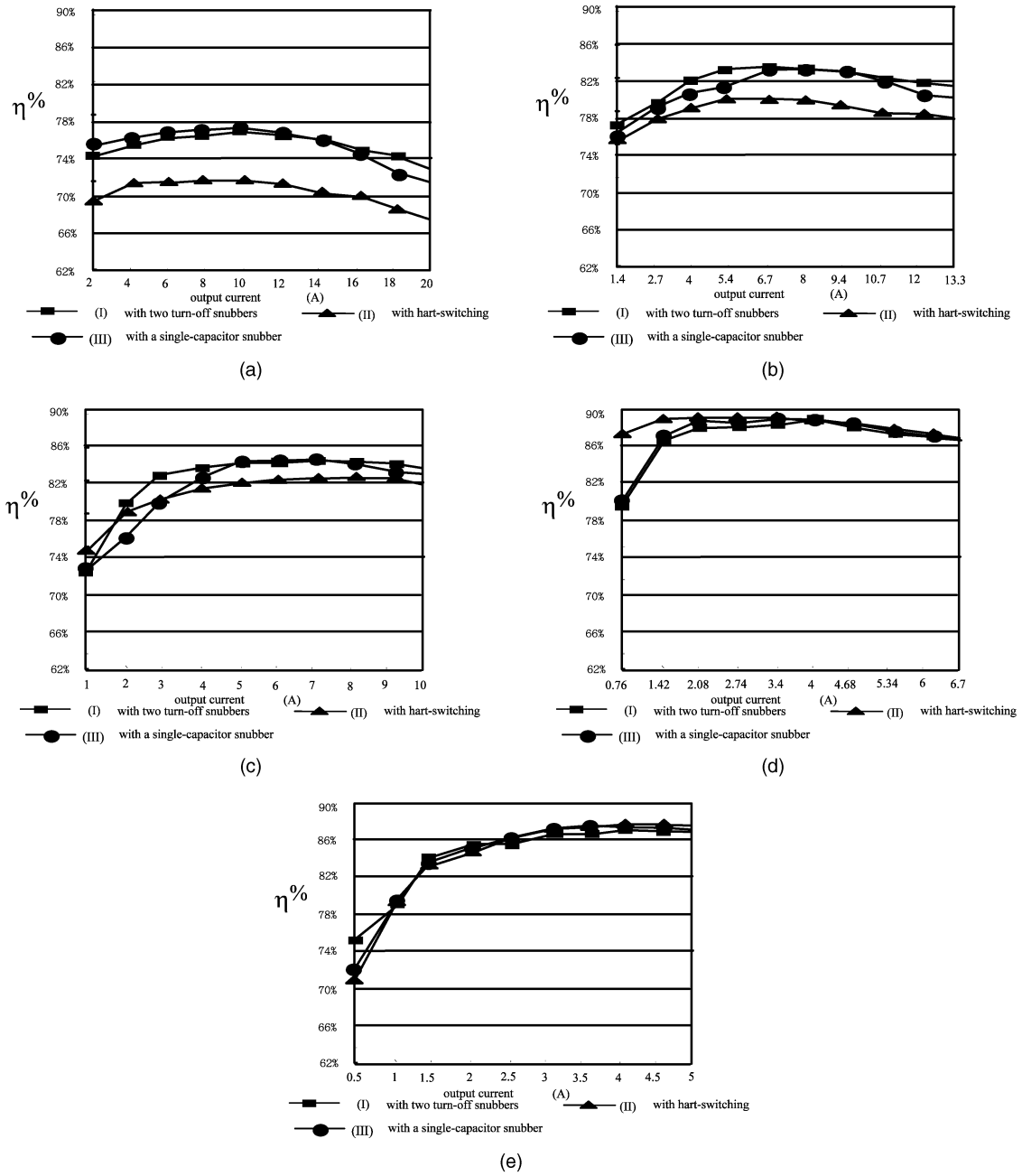


Fig. 19. Comparison among efficiencies of discussed interleaved buck converters with single-capacitor snubber, hard switching, and two turn-off snubbers at output voltages of (a) 12 V, (b) 18 V, (c) 24 V, (d) 36 V, (e) 48 V.

through the low impedance-path capacitor C_1, it will dominate the diode current I_{D2}, inducing switching loss $W_{S\,\mathrm{on}}$ at switch turn-on transition. However, if this switching loss is lower than the conduction loss due to diode D_2 during its freewheeling interval, the overall system efficiency still can be further improved, since the current originally flows through diode D_2 will be redirected to I_{DS2}.

VII. CONCLUSIONS

In this paper, interleaved buck converters with a single-capacitor snubber to smooth out switch turn-off transition have been proposed. Their operational principle, steady-state analysis, and design consideration have been described in detail and comparison among various performance aspects have been presented. The proposed soft-switching converters are using less number of component counts. Additionally, it has been found that the proposed converters have almost the same dynamic performance as their counterparts. In particular, from the efficiency comparison, it has been shown that the proposed converters can yield higher efficiency than their hard-switching counterparts at low output-voltage applications. An experimental prototype for a

TABLE I
Parameters for Calculating Switching and Conduction Losses

Parameter	Value
$t_{s\text{off}}$	80 ns
$t_{s\text{on}}$	120 ns
R_{ds}	0.07 Ω
L_1	40 μH
C_1	33 nF
T_s	20 μs

Peltier-device application (240 W, 24 Vdc/10 A) has been built and evaluated, achieving the efficiency of 83.2% at the full load condition and verifying feasibility of the proposed converters.

TABLE II
Performance Comparison Among Interleaved Buck Converters with Hard-Switching, Two Turn-Off Snubbers and Single-Capacitor Snubber

Type of Converters	Performance		
	Component Count		Efficiency (V_o = 24 V and P_o = 200 W)
	Buck	Snubber	
With hard switching (no snubber)	Coupled inductor: 1 MOSFET: 2 Diode: 2	Do not need extra component	82.5%
With two turn-off snubbers	Coupled inductor: 1 MOSFET: 2 Diode: 2	Inductor: 2 Capacitor: 4 Diode: 6	84.3%
With a single-capacitor snubber	Coupled inductor: 1 MOSFET: 2 Diode: 2	Capacitor: 1	84.0%

REFERENCES

[1] Liu, K-H., Oruganti, R-O., and Lee, F-C. (1995) Resonant switches—topologies and characteristics. In *Proceedings of the power Electronics Specialists Conference*, 1995, 62–67.

TABLE III
Power Loss Comparison Among Interleaved Buck Converters with Hard-Switching, Two Turn-Off Snubbers and Single-Capacitor Snubber

	Type of Converters	Power Loss				
		Calculated Results		Measured Results		
		Loss	Efficiency Reduction (V_o = 24 V and P_o = 200 W)	Loss	Efficiency Reduction (V_o = 24 V and P_o = 200 W)	Efficiency (V_o = 24 V and P_o = 200 W)
Conduction loss	With hard switching (no snubber)	0.7 W	0.3%	1 W	0.3%	
	With two turn-off snubbers	0. 95 W	0.4%	1.28 W	0.45%	
	With a single-capacitor snubber	0.8 W	0.33%	1.15 W	0.4%	
Switching loss	With hard switching (no snubber)	7.8 W	3.2%	13.97 W	4.76%	
	With two turn-off snubbers	0 W	0%	8.1 W	2.82%	
	With a single-capacitor snubber	5.48 W	2.3%	8.76 W	3.04%	
Total loss	With hard switching (no snubber)	8.5 W	3.5%	14.97 W	5.1%	82.5%
	With two turn-off snubbers	0.95 W	0.4%	9.38 W	3.3%	84.3%
	With a single-capacitor snubber	6.28 W	2.63%	9.91 W	3.4%	84.0%

[2] Zheng, T., Chen, D-Y., and Lee, F-C. (1986)
Variations of qusai-resonant dc-dc converter topologies.
In *Proceedings of the power Electronics Specialists Conference*, 1986, 381–392.

[3] Maksimovic, D., and Cuk, S. (1989)
A general approach to synthesis and analysis of quasi-resonant converter.
In *Proceedings of the power Electronics Specialists Conference*, 1989, 713–727.

[4] Tabiaz, W., and Lee, F-C. (1988)
Zero-voltage-switching multi-resonant technique: A novel approach to improve performance of high frequency qusai-resonant converters.
In *Proceedings of the Power Electronics Specialists Conference*, 1988, 9–17.

[5] Lee, F-C., Tabisz, W-A., and Jovanovic, M-M. (1989)
Recent developments in high-frequency qusai-resonant and multi-resonant converter topologies.
In *Proceedings of the third European Conference on Power Electronics and Applications*, 1989, 401–410.

[6] Liu, K-H., and Lee, F-C. (1990)
Zero-voltage switching technique in dc/dc converter.
IEEE Transactions on Power Electronics, **5** (July 1990), 9–17.

[7] Smith, K., and Smedley, K. (1999)
Properties and synthesis of lossless, passive soft switching PWM converters.
IEEE Transactions on Power Electronics, **14** (Sept. 1999), 890–899.

[8] Smith, K., and Smedley, K. (1997)
Lossless passive soft switching methods for inverters and amplifiers.
In *Proceedings of the Power Electronics Specialists Conference*, 1997, 1431–1439.

[9] Tseng, C-J., and Chen, C-L. (1998)
Passive lossless snubbers for dc/dc converters.
In *Proceedings of the Applied Power Electronics Conference*, 1998, 1049–1054.

[10] Yaakov, S-B., and Ivensky, G. (1997)
Passive lossless snubbers for high frequency PWM converters.
Tutorial of IEEE Power Electronics Specialists Conference, 1997.

[11] Munoz, C. (1998)
Study of a new passive lossless turn-off snubber.
In *Proceedings of the CIEP Conference*, 1998, 147–152.

[12] Watson, R., Hua, G., and Lee, F-C. (1996)
Characterization of an active clamp flyback topology for power factor correction applications.
IEEE Transactions on Power Electronics, **11** (Jan. 1996), 191–198.

[13] Duarte, C., and Barbi, I. (1997)
A family of ZVS-PWM active-clamping dc-to-dc converters: synthesis, analysis, design, and experimentation.
IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, **44** (Aug. 1997), 698–704

[14] Wong, P-L., et al. (2000)
Investigating coupling inductors in the interleaving QSW VRM.
In *Proceedings of the Applied Power Electronics Conference and Exposition*, 2000, 973–978.

[15] Wong, P-L., et al. (2001)
Performance improvements of interleaving VRMs with coupling inductors.
IEEE Transactions on Power Electronics, **16** (July 2001), 499–507.

[16] Chang, C. (1996)
Current ripple bounds of interleaved power converters.
IEEE Transactions on Aerospace and Electronic Systems, **32** (Oct. 1996), 1505–1508.

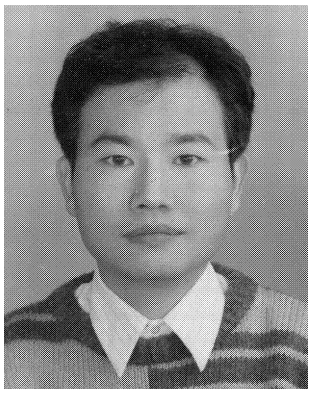
Yaow-Ming Chen (S'96—M'98) received the B.S. degree from the National Cheng-Kung University, Taiwan, and the M.S. and Ph.D. degrees from the University of Missouri, Columbia, in 1989, 1993, and 1997, respectively, all in electrical engineering.

From 1997 to 2000, he was with the I-Shou University, Taiwan, as an assistant professor. In 2000, he joined the National Chung-Cheng University, Taiwan, where he is currently an assistant professor of the Department of Electrical Engineering. His research interests include power electronic converters, power system harmonics and compensation, and intelligent control.

Dr. Chen is a member of the IEEE Power Electronics and Industrial Electronics Societies.

Sheng-Yu Tseng was born in Taiwan in 1970. He received the B.S. degree in electrical engineering from National Taipei University of Technology, Taipei, Taiwan, ROC, and the M.S. degree in electrical engineering from National Chung-Cheng University, Chia-Yi, Taiwan, in 1992 and 1999, respectively. He is currently a Ph.D. candidate in the Department of Electrical Engineering, National Chung-Cheng University, Chia-Yi, Taiwan.

His research interests include design of switching-mode power supplies, color plasma display panel driving circuits and pulsed voltage generator for transdermal drug delivery or processing microbes.



Cheng-Tao Tsai was born in Taiwan in 1962. He received the B.S. degree in electrical engineering from Feng Chia University, Taiwan, ROC, in 1991, and the M.S. degree in electrical engineering from National Chung Cheng University, in 2003. He is currently a Ph.D. candidate in the Department of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan.

His research interests include design of switching-mode power supplies, power factor correction technology and chargers for electric vehicle.

Tsai-Fu Wu (S'89—M'91—SM'98) received the B.S. degree in electronics engineering from National Chiao-Tung University, Taiwan, ROC, in 1983, the M.S. degree in electrical and computer engineering from Ohio University, OH, in 1988, and the Ph.D. degree in electrical engineering and computer science from University of Illinois, Chicago, in 1992.

From 1985 to 1986 he was a system engineer at SAMPO, Inc., Taiwan, developing and designing graphic terminals. He was a teaching and research assistant in the Department of Electrical Engineering and Computer Science, University of Illinois, Chicago from 1988 to 1992. Since 1993, he has been with the Electrical Engineering Department, National Chung Cheng University, Taiwan, where he is currently a professor and the director of the Power Electronics Applied Research Laboratory (PEARL). His research interests include developing and modeling of power converters, design of electronic dimming ballasts for fluorescent lamps, metal halide lamps and plasma display, and design of solar-panel-supplied inverters for grid connection.

Dr. Wu is a senior member of the CIE.