An Active-Clamp Push–Pull Converter for Battery Sourcing Applications

Tsai-Fu Wu, *Senior Member, IEEE*, Jin-Chyuan Hung, *Member, IEEE*, Jeng-Tsuen Tsai, Cheng-Tao Tsai, and Yaow-Ming Chen, *Senior Member, IEEE*

***Abstract*—This paper presents an active-clamp push–pull converter for battery sourcing applications. A pair of auxiliary switches, resonant inductors, and clamping capacitors is added to the primary side of the transformer to clamp voltage spike and recycle the energy trapped in the leakage inductors. In the proposed active-clamp push–pull converter, since both main and auxiliary switches can be turned ON with zero-voltage switching, switching loss can be reduced and conversion efficiency therefore can be improved significantly. Furthermore, the proposed converter can eliminate potential flux-imbalance problems existing in the conventional push–pull converter. In this paper, a 1 kW active-clamp push–pull converter was implemented, from which experimental results have shown that efficiency improvement and surge suppression can be achieved effectively. It is relatively feasible for applications to battery sourcing converters.**

***Index Terms*—Active clamp, push–pull converter, zero-voltage switching (ZVS).**

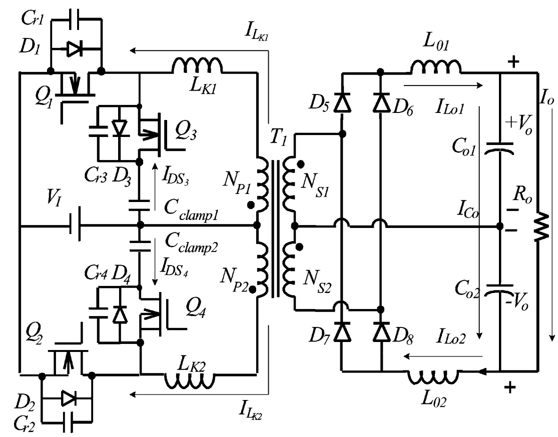


Fig. 1. Schematic diagram of the proposed push–pull converter with active-clamp circuits.

I. Introduction

BATTERY souring applications include mostly a lot of uninterruptible power supplies (UPSs), which have been used broadly to supply clean and uninterrupted power to loads. In UPS applications, they need dischargers to draw power from batteries. In practice, the voltage level of batteries is usually much lower than that of dc-link bus; thus, a converter with a high step-up voltage ratio is required for the dischargers. Furthermore, to effectively utilize the energy stored in batteries, the dischargers should be designed with high efficiency.

To achieve a high step-up voltage ratio, a common solution is using a push–pull converter [1]. However, leakage inductor of the transformer would induce voltage spike that results in high component stress, low conversion efficiency, and high noise level. The other drawback of a push–pull converter is the flux-imbalance problem [1]. To alleviate these drawbacks, several kinds of soft-switching push–pull converters have been proposed in literature [2]–[7]. The resonant push–pull converters have been presented in [2]–[4], which can achieve zero-voltage switching (ZVS) to increase conversion efficiency, while their component stress and circulation energy are still high. In addition, the converters are regulated by variable frequency control, and it is difficult to design optimal filters, which would increase cost and control complexity. To release these problems, the ZVS push–pull converters were proposed in [5], [6]. These converters with two synchronous switches in the secondary circuits provide the ZVS opportunity for all of the active switches. Although these converters present the advantages of a pulse-width modulation (PWM) control and high efficiency, their active switches are located both on the primary and the secondary sides of the transformer, increasing their driving complexity and cost. In [7], two active-clamp circuits are added to the primary side of the transformer for recycling leakage energy and limiting the voltage spike. In the converter, the clamping circuits can also achieve the ZVS, which makes the converter more viable. However, since its active-clamp circuits are a boost type, voltage stresses imposed on the active switches are much higher than twice the input voltage. Thus, the component stress has not been minimized yet. In this paper, a buck-boost type of active-clamp circuits is proposed, and voltage stresses of the active switches can be limited to twice the input voltage, reducing the component stress significantly. The proposed converter is depicted in Fig. 1.

In the paper, operational principle of the proposed converter is described in Section II. Section III presents the steady-state analysis of the converter, from which design procedure is summarized. Experimental results obtained from a prototype

Paper IPCSD-07-059, presented at the 2005 IEEE Applied Power Electronics Conference and Exposition, Austin, TX, March 6–10, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review April 3, 2005 and released for publication July 11, 2007.

T.-F. Wu, C.-T. Tsai, and Y.-M. Chen are with the Elegant Power Application Research Center (EPARC), Department of Electrical Engineering, National Chung Cheng University, Chia-Yi 621, Taiwan, R.O.C. (e-mail: tfwu@ee.ccu.edu.tw; chioushu@ms41.hinet.net; ieeymc@ccu.edu.tw).

J.-C. Hung and J.-T. Tsai are with NuLight Technology Corporation, Tainan 741, Taiwan, R.O.C. (e-mail: hung@nlt.com.tw; smilearmy2001@yahoo.com.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIA.2007.912748

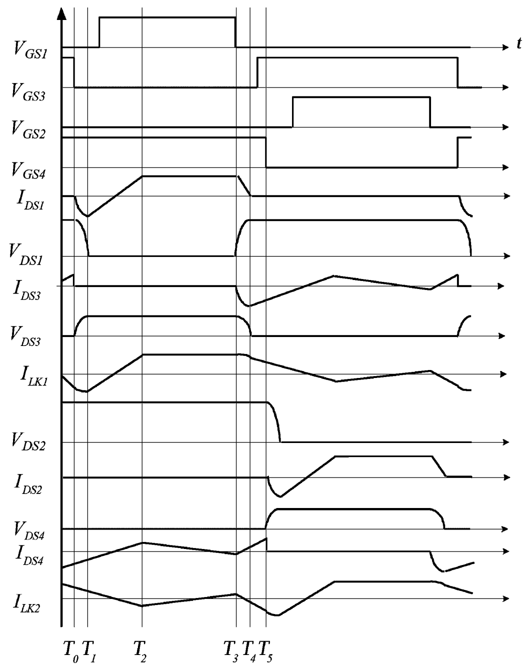


Fig. 2. Driving signals and current and voltage waveforms of the key components in the proposed converter.

built with the proposed converter are presented in Section IV to verify its feasibility. Finally, the paper is concluded in Section V.

II. Operation of the Proposed Push–Pull Converter

As shown in Fig. 1, the proposed converter consists of the following components: two main switches Q_1 and Q_2, a center-tapped transformer T_1, four output rectifier diodes D_5–D_8, two output filter inductors L_{O1} and L_{O2}, two sets of clamping circuits, and two output filter capacitors C_{O1} and C_{O2}. The clamping circuits are composed of two auxiliary switches Q_3 and Q_4, leakage inductors L_{K1} and L_{K2} of the transformer, two clamping capacitors C_{clamp1} and C_{clamp2} and snubbers C_{r1}–C_{r4} that can limit the rising rate of voltage, reducing turn-OFF loss significantly. Switches Q_1 and Q_3, as well as Q_2 and Q_4, are driven in an asymmetrical complementary manner with a dead time to achieve ZVS.

The driving signals and current and voltage waveforms of key components are shown in Fig. 2. When Q_1 is turned ON while Q_3 is turned OFF, the current flows through L_{K1}, Q_1 and winding N_{P1}, which will couple a current to the secondary side and flow through $N_{S1}, N_{S2}, D_5, D_8, L_{O1}$, and L_{O2} to the load. When Q_1 is turned OFF while Q_3 is turned ON, leakage inductor L_{K1} will resonate with capacitors C_{r1} and C_{r3}. When the voltage across C_{r3} drops to zero, D_3 is forced to forward bias, and then, the energy trapped in the leakage inductor is recycled to C_{clamp1}. After a quarter of the resonant period of L_{K1} and C_{clamp1}, capacitor C_{clamp1} begins to release its stored energy through Q_3, L_{K1} and the transformer to the load. It is worth mentioning that flux balance can be always insured because the clamping circuits help to reset the core and recycle the trapped energy back to the source during the clamping period.

To simplify description of the operational modes, the following assumptions are made.

1) Capacitance of $C_{\text{clamp1}}, C_{\text{clamp2}}$, or C_O is large enough so that the voltages across them can hold constant over a switching period.
2) Capacitance of C_{clamp1} and that of C_{clamp2} are identical, and inductance of L_{LK1} and that of L_{LK2} are identical.
3) All of the switching devices, MOSFETs and diodes, are ideal.

Based on the aforementioned assumptions, operation of the proposed converter over a half switching period can be divided into five modes. Fig. 3 shows the topological modes of the proposed converter over half the switching cycle, and Fig. 2 shows its key conceptual voltage and current waveforms. The operation of the converter is explained mode by mode as follows.

Mode 1 [Fig. 3(a), $T_0 \le t < T_1$]: At T_0, auxiliary switch Q_3 is turned OFF while Q_4 is still conducting. In this mode, leakage inductor L_{K1} resonates with C_{r1} and C_{r3}. Capacitor C_{r3} is continuously charged toward $V_{\text{Clamp1}} + V_I$, while capacitor C_{r1} is discharged down to zero. To achieve an ZVS feature for switch Q_1, the energy trapped in leakage inductor L_{K1} should satisfy the following inequality:

$$0.5 \times [i_{LK1}(T_0)]^2 L_{LK1} \ge 0.5 \times [v_{DS1}(T_0)]^2 (C_{r1}//C_{r3}). \tag{1}$$

During this mode, inductor L_{K2} keeps to release its stored energy through D_4 to the capacitor C_{clamp2}. On the secondary side of the transformer, rectifier diodes D_5–D_8 begin to freewheel.

Mode 2 [Fig. 3(b), $T_1 \le t < T_2$]: Mode 2 starts with voltage v_{DS1} dropping to zero at T_1. Inductor current i_{LK1} forces the body diode D_1 conducting and creating an ZVS condition for Q_1. The driving signal should be applied to Q_1 at this time interval to achieve an ZVS feature. Inductor current $i_{LK1}(t)$ increases linearly, which can be expressed as follows:

$$i_{LK1}(t) = i_{LK1}(T_1) + \frac{V_I}{L_{K1}} t. \tag{2}$$

When inductor current $i_{LK1}(t)$ goes beyond the zero level, Q_1 can be turned ON with the ZVS.

Meanwhile, leakage inductor L_{K2} releases its trapped energy continuously to clamping capacitor C_{clamp2}. The inductor current $i_{LK2}(t)$ can be expressed as follows

$$i_{LK2}(t) = i_{LK2}(T_1) + \frac{-V_{C_{\text{clamp2}}}}{L_{LK2}} t. \tag{3}$$

On the secondary side of the transformer, rectifier diodes D_5–D_8 are freewheeling. This mode ends when $i_{LK1}(t)$ reaches the reflected current of the output inductor current i_{Lo1}.

Mode 3 [Fig. 3(c), $T_2 \le t < T_3$]: At T_2, the converter starts to transfer power from the input through the transformer to the load, and diodes D_6 and D_7 tend to be reversely biased. Inductor L_{K1} is linearly charged while inductor L_{K2} is still releasing its trapped energy to C_{clamp2}. Then, capacitor

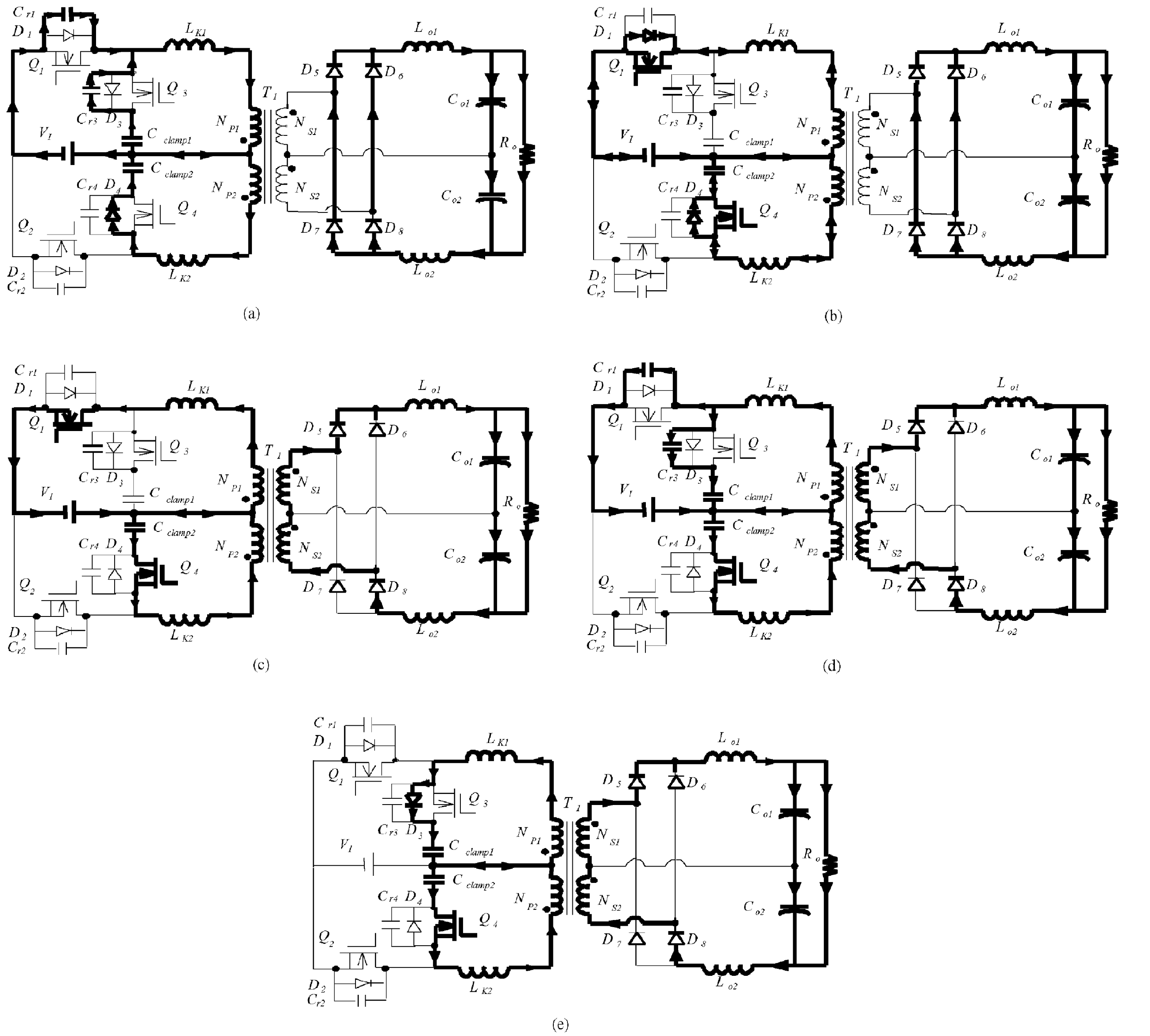


Fig. 3. Topological modes existing in the proposed converter operation over half a switching cycle.

C_{clamp2} begins to release its trapped energy through Q_4, L_{K2}, and the transformer to the load. Inductor currents $i_{LK1}(t)$ and $i_{LK2}(t)$ can be expressed as follows

$$i_{LK1}(t) = i_{LK1}(T_2) + \frac{(V_I - V_{Np1})}{L_{LK1}} t \tag{4}$$

and

$$i_{LK2}(t) = i_{LK2}(T_2) + \frac{-(V_{C_{\mathrm{clamp2}}} + V_{Np2})}{L_{LK2}} t \tag{5}$$

where V_{Np1} and V_{Np2} are the voltages across the windings N_{P1} and N_{P2}, respectively. On the secondary side of the transformer, the current flows through the paths of N_{S1}–D_5–L_{O1}–C_{O1} and N_{S2}–D_8–C_{O2}–L_{O2}. Inductor currents i_{Lo1} and i_{Lo2} are linearly increased, which can be expressed as follows:

$$i_{Lo1}(t) = \frac{n(V_I - v_{LK1}) - 0.5V_O}{L_{o1}} \times t + i_{Lo1}(T_2) \tag{6}$$

and

$$i_{Lo2}(t) = \frac{n(V_I - v_{LK1}) - 0.5V_O}{L_{o2}} \times t + i_{Lo2}(T_2) \tag{7}$$

where v_{LK1} is the voltages across L_{K1}, and $n = N_{S1}/N_{P1} = N_{S2}/N_{P2}$ is the secondary to the primary turns ratio of transformer T_1.

Mode 4 [Fig. 3(d), $T_3 \le t < T_4$]: At T_3, main switch Q_1 is turned OFF and auxiliary switch Q_3 still stays in the OFF state. In this mode, leakage inductor L_{K1} releases its energy to capacitors C_{r1} and C_{r3} with a resonant manner. Capacitor C_{r1} is charged toward $(V_I + V_{C_{\mathrm{clamp1}}})$, while capacitor C_{r3} is discharged down to zero. To achieve an ZVS feature for switch Q_3, the energy tapped in leakage inductor L_{K1} should satisfy the inequality

$$0.5 \times [i_{LK1}(T_3)]^2 L_{K1} \ge 0.5 \times [v_{DS3}(T_3)]^2 (C_{r1}//C_{r3}). \tag{8}$$

During this mode, capacitor C_{clamp2} continuously releases its stored energy. On the secondary side of the transformer, the current flows through the paths of N_{S1}–D_5–L_{O1}–C_{O1} and N_{S2}–D_8–C_{O2}–L_{O2}.

Mode 5 [Fig. 3(e), $T_4 \le t < T_5$]: Mode 5 starts with voltage v_{DS3} dropping to zero at T_4. Inductor current i_{LK1} forces the body diode D_3 conducting and creating an ZVS condition for Q_3. The driving signal should be applied to Q_3 at this time interval to achieve an ZVS feature. In this mode, the energy trapped in L_{K1} is recycled to C_{clamp1}. Due to the capacitance of C_{clamp1} is large enough, voltage V_{Clamp1} will hold constant. Inductor current i_{LK1} is linearly discharged, which can be expressed as follows:

$$i_{LK1}(t) = i_{LK1}(T_4) + \frac{-(V_{\mathrm{Clamp1}} + V_{Np1})}{L_{K1}} t. \tag{9}$$

During this mode, capacitor C_{clamp2} continuously releases its stored energy. On the secondary side of the transformer, the current flows through the paths of N_{S1}–D_5–L_{O1}–C_{O1} and N_{S2}–D_8–C_{O2}–L_{O2}. Mode 5 ends when auxiliary switch Q_4 is turned OFF.

When auxiliary switch Q_4 is turned OFF at the end of mode 5, operation of the other half switching cycle will start.

In the proposed converter, both of main and auxiliary active switches are operated with the ZVS, and the energy trapped in the leakage inductors can be recovered. With the clamping circuit, the main switches can be operated with low voltage spikes, reducing component stresses significantly. The proposed converter can reduce not only switching loss but also turns ratio of a transformer over a conventional push–pull converter. Detailed analysis and parameter design are presented in the following section.

III. Analysis and Design

A. Voltage Transfer Ratio and Clamped Voltage

In the steady-state operation of the proposed converter, the time intervals T_0 to T_1 and T_3 to T_4 are very short as compared to one switching period. Thus, they will not be considered in the analysis of dc voltage transfer ratio, and the simplified waveforms are shown in Fig. 4. In Fig. 4, the duty ratio *D* is the on time of main switch Q_1 or Q_2, and T_S represents the switching period of the converter operation. Since inductance of L_{K1} and L_{K2} is less than that of the magnetizing inductors of the center-tapped transformer, the voltages across L_{K1} and L_{K2} can be also neglected from the analysis.

According to the volt–second balance principle of the inductors, the voltages across C_{clamp1} and C_{clamp2} can be derived as follows:

$$V_{C_{\mathrm{clamp1}}} = V_{C_{\mathrm{clamp2}}} = V_{C_{\mathrm{clamp}}} = \frac{D}{1-D} V_I. \tag{10}$$

From (10), we can plot the relationship between voltage $V_{C_{\mathrm{clamp}}}$ and duty ratio *D* for different input voltages, as illustrated in Fig. 5. According to the plots, voltage $V_{C_{\mathrm{clamp}}}$ will go beyond input voltage V_I when *D* is greater than 0.5 that will result in a high voltage stress imposed on the components. Thus,

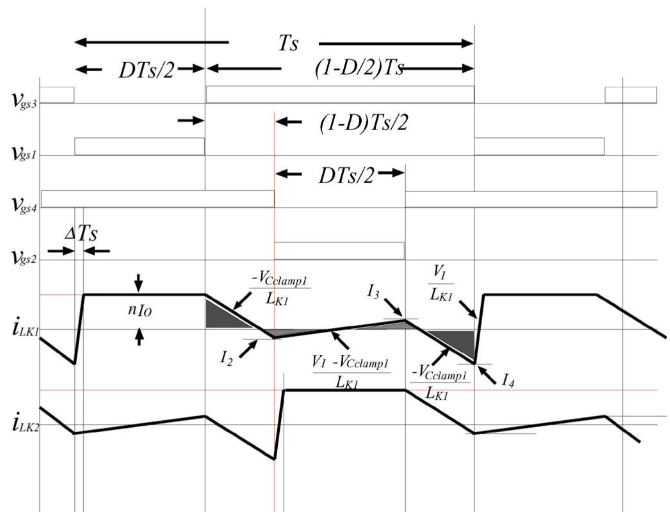


Fig. 4. Simplified key current and voltage waveforms of the proposed converter.

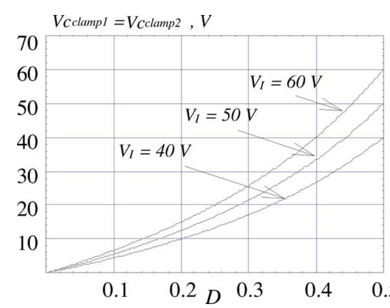


Fig. 5. Plots of voltages V_{Clamp1} and V_{Clamp2} versus duty ratio *D* for various input voltages.

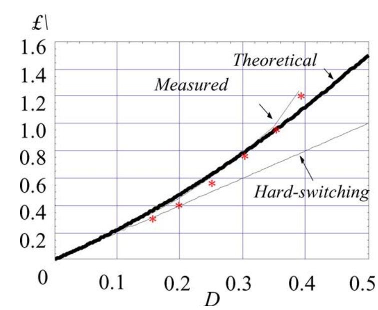


Fig. 6. Plots of normalized voltage ratio α versus duty ratio *D*.

the duty ratio is usually limited to being lower than 0.5 in the converter design. When ignoring the charging time of the leakage inductors, the input-to-output transfer ratio can be derived as

$$\frac{V_o}{V_I} = 2n(D + D^2) \tag{11}$$

where $n = N_{S1}/N_{P1} = N_{S2}/N_{P2}$. From (11), we can plot the curves showing the relationship between *D* and normalized input-to-output voltage ratio $\alpha = (V_O/V_I)/n$, as illustrated in Fig. 6. It can be observed from the curve denoted with "theoretical" that the proposed converter can yield a higher step-up voltage ratio than that of a conventional hard switching one.

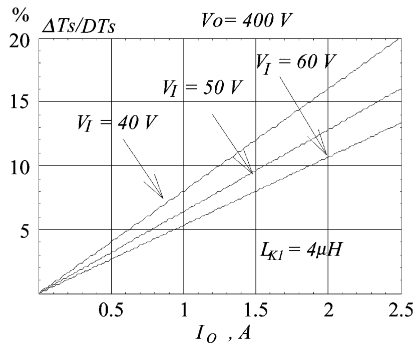


Fig. 7. Plots of normalized lost duty ratio $\Delta T_S/DT_S$ versus output current I_O for various input voltages.

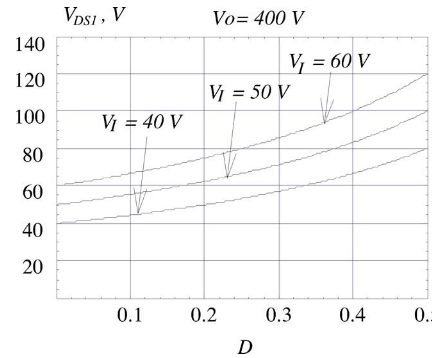


Fig. 8. Plots of voltage V_{DS1} versus duty ratio D for various input voltages.

Charging time of the leakage inductor will reduce the effective duty ratio. The lost duty time interval ΔT_S can be expressed as

$$\Delta T_S = \frac{2nI_O L_{K1}}{V_I} \tag{12}$$

where I_O is the average output current. During the charging time, there is no power delivered to the load. Thus, the input-to-output transfer ratio shown in (11) should be corrected to the expression

$$\frac{V_o}{V_I} = 2n\left[D - \frac{\Delta T_S}{T_S} + \left(D - \frac{\Delta T_S}{T_S}\right)^2\right]. \tag{13}$$

From (12), we can sketch the curves showing the relationship between normalized lost duty ($\Delta T_S/DT_S$) and I_O for different values of input voltage V_I, as illustrated in Fig. 7. The lost duty is proportional to the output current and leakage inductance, while it is inversely proportional to the input voltage. In the converter, leakage inductor L_{K1} is used for achieving the ZVS. Larger leakage inductance can achieve the ZVS over a wider load range. However, it will result in a larger duty loss and need a transformer with higher turns ratio, which in turn will result in low efficiency. Thus, the lost duty ratio in the proposed converter is a critical issue. In practice, the lost duty ratio should be limited to below 10% of the minimum duty ratio to ensure high efficiency and low current stress. Analytical expressions of the component stresses are derived in the following section.

B. Voltage and Current Stresses

According to the previous description of the operational modes, the voltages across main switches Q_1 and Q_2, auxiliary switches Q_3 and Q_4, and rectifier diodes D_5–D_8 can be derived as follows

$$V_{DS1} = V_{DS2} = V_I + V_{C_{\rm clamp}} \tag{14}$$

$$V_{DS3} = V_{DS4} = V_I + V_{C_{\rm clamp}} \tag{15}$$

and

$$V_{D5} = V_{D6} = V_{D7} = V_{D8} = 2V_O. \tag{16}$$

Applying amp–second balance principle to capacitors $C_{\rm clamp1}$ and $C_{\rm clamp2}$ can yield that two of the gray areas and two of the grid areas should be, respectively, identical in the steady state, as illustrated in Fig. 4. Thus, absolute values of the peak inductor current and its valley current will be identical. The averaged currents flowing through main switches Q_1 and Q_2, auxiliary switches Q_3 and Q_4, and diodes D_5–D_8 can be derived as

$$I_{DS1} = I_{DS3} = 2nI_O(D + D^2)/D \tag{17}$$

$$I_{DS3} = I_{DS4} = 0 \tag{18}$$

and

$$I_{D5} = I_{D6} = I_{D7} = I_{D8} = I_O/[2(D + D^2)]. \tag{19}$$

Their peak currents therefore can be expressed as

$$I_{DS1,PK} = I_{DS1} + \frac{1}{2}I_m \tag{20}$$

$$I_{DS2,PK} = I_{DS1,PK} \tag{21}$$

and

$$I_{D5} = I_{D6} = I_{D7} = I_{D8} = \frac{I_O}{2(D + D^2)} \tag{22}$$

where

$$I_m = \frac{V_I}{L_m}DT_S \tag{23}$$

and I_m is the magnetizing current of transformer T_1.

From (12)–(14), we can plot the curves showing the relationship between duty ratio D and component stress V_{DS1} for different values of input voltage V_I, as illustrated in Fig. 8. It can be observed that the voltage stresses of Q_1–Q_4 are increased with increase of D.

In the converter with the active-clamp circuits, both the voltage stresses of the main switches and auxiliary switches can be reduced. Lower switch voltage stress implies that switches with lower r_{ds}(ON) can be used. Moreover, the trapped energy in the leakage inductor can be recovered. It is notable that the problem results from voltage spike can be eliminated in the proposed converter.

In the conventional push–pull converter, a potential problem of flux imbalance will limit its applications. The active-clamp circuits adopted in the converter can eliminate this problem, which is explained as follows. In practice, a real circuit would have different duty ratios for the main switches, which will

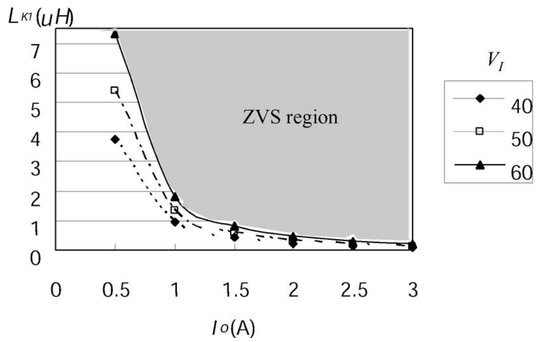


Fig. 9. Plots of the ZVS region relating to L_{K1} and I_o at $V_I = 60$ V.

result in different magnetizing as well as leakage inductor currents. Since the leakage inductor currents will be recycled to the clamping capacitor, a larger current will result in more charges stored in the clamping capacitor. Then, the capacitor voltage will increase. The increase of the clamping capacitor voltage will in turn provide a larger product of volt–second that can be used to balance the excessive flux inducing from a larger duty ratio. The volt–second and amp–second balances in the leakage inductors, transformer, and clamping capacitors can always hold in the steady state. Thus, with the active-clamp circuits, potential flux-imbalance problems can be solved. Furthermore, the active-clamp circuits can help to achieve the ZVS features. The condition for achieving the ZVS is derived in the following section.

C. Condition for ZVS

According to (1) and (8), it is necessary to store enough energy in the leakage inductor to achieve the ZVS at switch turn-ON transition. Because the ZVS transient period of switch Q_1 is less than that of switch Q_3, the ZVS condition for both active switches should be determined by (1). From, (1), (14), (17), (20), and (23), we can obtain the inequality

$$L_{K1} = L_{K2} \geq \frac{(C_{r1}//C_{r3})(V_I - V_{C_{\mathrm{clamp}}})^2}{(I_{DS1} + I_m)^2} \tag{24}$$

which can be used to determine a proper leakage inductor. According to (24), the ZVS condition for the switches is depending on (C_{r1}//C_{r3}), L_{K1}, V_I, and I_O. The parasitic capacitors C_{r1} and C_{r3} of the power MOSFETs are used as the resonant capacitors in the proposed converter. For determining leakage inductance, we can plot the curves showing the relationship between leakage inductance L_{K1} and output current I_O under different input voltages, as illustrated in Fig. 9. The inductance should be selected from the gray area for achieving the ZVS. From Fig. 9, it can be seen that the ZVS region of the proposed converter will shrink with increase of input voltage and decrease of output current.

D. Summary of Design Procedure

Based on the equations and curves discussed previously, a design procedure of the proposed converter is summarized as follows.

1) From the specifications of the input low-line voltage $V_I = V_{I(\mathrm{low})}$ and the output voltage V_O, a maximum duty ratio $D = D_{\max} < 0.5$ is selected, and then, an appropriate normalized voltage ratio α can be determined from the curves shown in Fig. 6 (a larger value of D will result in lower current stress).
2) According to the determined α and the input high-line voltage $V_I = V_{I(\mathrm{high})}$, the minimum duty ratio $D = D_{\min}$ can be read from the curves shown in Fig. 6.
3) According to the determined α and the specified input voltage, turns ratio n can be calculated from (9).
4) According to the determined n and $D_{\min}$, V_{DS1} and v_{DS3} can be determined from (14) and (15).
5) Verify if the voltage stresses of V_{DS1} and v_{DS3} are below the rated voltage of the MOSFETs. If it is not, decrease the values of turns ratio n, and repeat steps 1–4.
6) From Fig. 9 and the minimum output current for achieving the ZVS, the leakage inductor can be determined.

IV. Experimental Results

To illustrate the analysis and discussion, a 1 kW prototype of a discharger with active-clamp circuits was built. The schematic diagram of the proposed converter is depicted in Fig. 1 and its specifications are listed as follows:

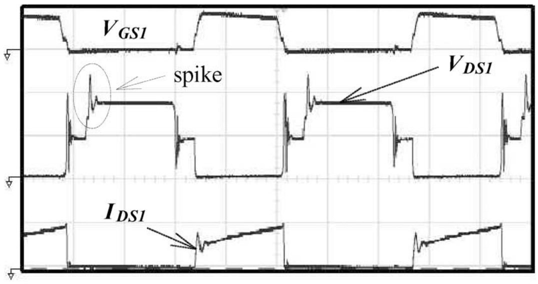
1) input voltage: 40–60 V_{DC};
2) output voltage: 400 V_{DC};
3) output current: 2.5 A;
4) switching frequency: 50 kHz.

With these specifications and choosing $D_{\max} = 0.42$, normalized voltage ratio $\alpha = 1.2$ can be determined from Fig. 6. According to the determined $\alpha = 1.2$ and the low-line voltage $V_I = 40$ V, turns ratio $n = 8$ can be determined from (11). Voltage stress $V_{DS1} = 100$ V of switch Q_1 and voltage stress $v_{DS3} = 100$ V of switch Q_3 can be determined from (14) and (15), respectively. If the minimum output current is limited to 0.75 A for achieving an ZVS condition, the leakage inductor can be then determined as 4 μH from Fig. 9. Although the ZVS does not sustain at the load current below 0.75A, it will not cause thermal problems at converter operation.

The components of the power stage are designed as follows:

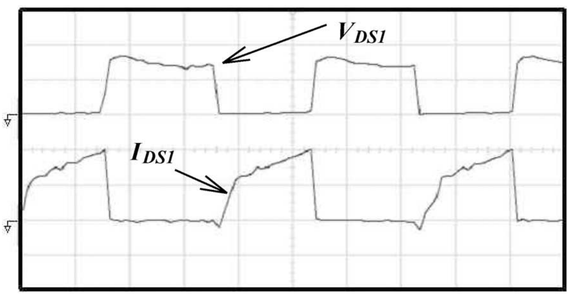
1) Q_1, Q_2: IRFP260;
2) D_5–D_8: HFA08TB120;
3) Q_3, Q_4: FB61N15D;
4) $C_{\mathrm{clamp1}}, C_{\mathrm{clamp2}}$: 2.2 μF/200 V;
5) L_{m1}, L_{m2}: 35 μH, 35 μH;
6) C_{O1}, C_{O2}: 470 μF/250 V;
7) L_{K1}, L_{K2}: 4 μH, 4 μH;
8) L_{O1}, L_{O2}: 600 μH, 600 μH;
9) T_1: TDK EE55; $N_{P1} = N_{P2} = 4$ T; $N_{S1} = N_{S2} =$32 T.

Fig. 10 shows the measured waveforms from a push–pull converter without clamping circuit to illustrate high voltage spike across the active switch. Figs. 11 and 12 show measured waveforms of drain–source voltage and current to illustrate low voltage stress and no spike at switches Q_1 and Q_3. Figs. 13 and 14 show measured waveforms of drain–source voltage and current to illustrate an ZVS feature. Fig. 15 shows efficiency



(V_{GS1}: 20 V/div, V_{DS1}: 50 V/div, I_{DS1}: 20 A/div, Time: 5µs/div).

Fig. 10. Measured waveforms of gate signal V_{GS1}, drain–source voltage V_{DS1} and current I_{DS1} from converter without active-clamp circuits illustrating high voltage spike across Q_1.

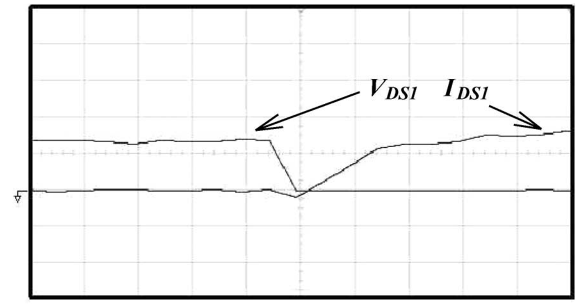


(V_{DS1}: 50 V/div, I_{DS1}: 10 A/div, Time: 5µs/div).

Fig. 11. Measured waveforms of drain–source voltage V_{DS1} and current I_{DS1} from the proposed converter illustrating a low voltage stress and no spike at switch Q_1.

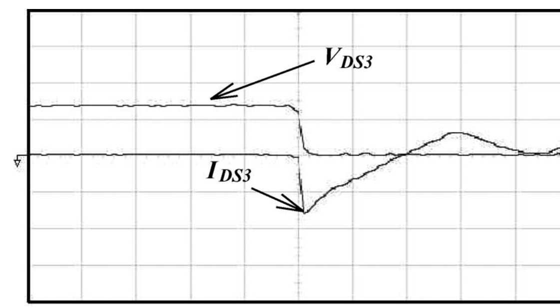
(V_{DS3}: 50 V/div, I_{DS3}: 10A/div, Time: 5µs/div).

Fig. 12. Measured waveforms of drain–source voltage V_{DS2} and current I_{DS2} from the proposed converter illustrating a low voltage stress and no spikes at switch Q_3.



(V_{DS1}: 50 V/div, I_{DS1}: 10 A/div, Time: 5µs/div).

Fig. 13. Measured waveforms of drain–source voltage V_{DS1} and current I_{DS1} illustrating an ZVS feature.



(V_{DS3}: 50 V/div, I_{DS3}: 10A/div, Time: 5µs/div).

Fig. 14. Measured waveforms of drain–source voltage V_{DS2} and current I_{DS2} illustrating an ZVS feature.

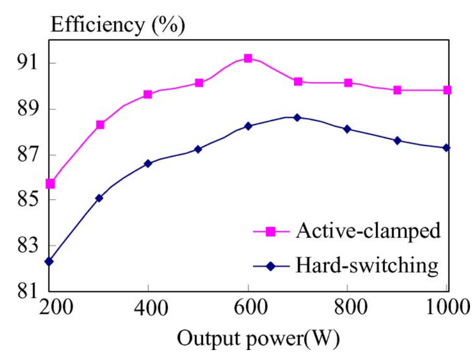


Fig. 15. Plots of efficiency versus power for the proposed converter and the hard switching without the active-clamp circuits.

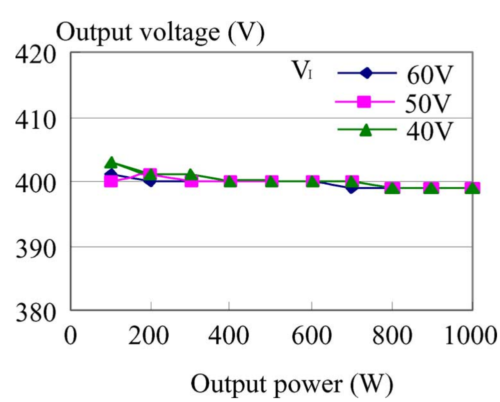


Fig. 16. Output voltage plots of the proposed converter under input and load variations illustrating a tight output regulation.

measurements from the proposed converter and a hard switching one, from which it can be seen that efficiency has been improved significantly and the maximum efficiency can reach 91%. Fig. 16 shows measurements of output voltage under input and load variations, from which it can be observed that tight regulation can be achieved.

Measured results from a hard switching and the proposed push–pull converters are listed in Tables I and II. Tables III and IV summarize their loss analysis results. In Table III, the total loss of MOSFET switching loss, diode switching loss, and snubber loss is 51.62 W. This significant loss can be reduced when the active-clamp circuits are adopted. Even though the active-clamp circuits used to achieve the ZVS cause extra conduction loss (∼4.64 W), the overall power loss is still far below that of

TABLE I
MEASURED RESULTS FROM A HARD-SWITCHING PUSH–PULL CONVERTER

Items / P_I (W)	V_I (V)	I_I (A)	P_O (W)	Conversion efficiency (%)
243	40	6.07	200	82.3
352.5	40	8.81	300	85.1
461.9	40	11.57	400	86.6
574.1	40	14.35	500	87.1
680.3	40	17.00	600	88.2
802.8	40	20.07	700	87.2
908.1	40	22.70	800	88.1
1027.4	40	25.68	900	87.6
1160.5	40	29.00	1000	86.2

TABLE II
MEASURED RESULTS FROM THE PROPOSED PUSH–PULL CONVERTER WITH ACTIVE-CLAMP CIRCUITS

Items / P_I(W)	V_I (V)	I_I (A)	P_O (W)	Conversion efficiency (%)
235.5	40	5.88	200	84.9
341.8	40	8.55	300	87.7
448.6	40	11.22	400	89.2
559.1	40	13.97	500	89.4
657.0	40	16.42	600	91.3
779.7	40	19.49	700	89.8
887.9	40	22.19	800	90.1
1002	40	25.05	900	89.8
1113.5	40	28.37	1000	89.8

TABLE III
LOSS ANALYSIS OF A HARD-SWITCHING PUSH–PULL CONVERTER AT 1 KW

Items of losses	**Loss (W)**	**%**
MOSFET, conduction loss	57.80	36.19
MOSFET, switching loss	19.64	12.27
Diode, conduction loss	11.66	7.29
Diode, switching loss	16.80	10.50
Transformer, core loss	10.50	6.56
Transformer, copper loss	4.68	2.93
Snubber	15.18	9.49
others	23.63	14.77
Total losses	**160**	**100**

TABLE IV
LOSS ANALYSIS OF THE PROPOSED PUSH–PULL CONVERTER AT 1 KW

Items of losses	**Loss (W)**	**%**
MOSFET, conduction loss (two main MOSFETs and two active-clamp MOSFETs)	62.44	55.66
MOSFET, switching loss	~0	0
Diode, conduction loss	11.67	10.33
Diode, switching loss	~0	0
Transformer, core loss	10.50	9.29
Transformer, copper loss	4.68	4.14
Snubber	0	0
others	23.63	20.58
Total losses	**113**	**100**

its hard-switching counterpart. Conversion efficiency has been improved significantly in the proposed converter.

V. CONCLUSION

This paper has proposed a push–pull converter with active-clamp circuits. In the paper, analysis of the converter has been presented in detail, from which design equations and circuit parameters were derived. The proposed converter can be operated with constant switching frequency and PWM control. By adopting the active-clamp circuits, energy trapped in the leakage inductors can be recovered, the ZVS features can be achieved, and voltage spike can be suppressed effectively. Moreover, potential flux-imbalance problems with the transformer can be eliminated from the proposed converter. Experimental results have verified that the proposed converter can achieve high efficiency over a wide load range. It is relatively feasible for high step-up discharger applications.

REFERENCES

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2001, pp. 159–160.
[2] M. J. Ryan, W. E. Brumsickle, D. M. Divan, and R. D. Lorenz, “A new ZVS LCL-resonant push–pull DC–DC converter topology,” *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1164–1174, Sep./Oct. 1998.
[3] I. Boonyaroonate and S. Mori, “A new ZVCS resonant push–pull DC/DC converter topology,” in *Proc. Appl. Power Electron. Conf.*, 2002, pp. 1097–1100.
[4] J. Ying, Q. Zhu, H. Lin, and Z. Wu, “A zero-voltage-switching (ZVS) push–pull DC/DC converter for UPS,” in *Proc. IEEE Power Electron. Drive Syst. Conf.*, 2003, pp. 1495–1499.
[5] M. Shoyama and K. Harada, “Zero-voltage-switched push–pull DC–DC converter,” in *Proc. Power Electron. Spec. Conf.*, 1991, pp. 223–229.
[6] M. Shoyama and K. Harada, “Zero-voltage-switching realized by magnetizing current of transformer in push–pull current-fed DC–DC,” in *Proc. Power Electron. Spec. Conf.*, 1993, pp. 178–184.
[7] R. Torrico-Bascope, F. L. M. Antunes, and I. Barbi, “Optimal double ZVS-PWM active-clamping forward converter with inputs connected in series and parallel,” in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 1621–1626.

Tsai-Fu Wu (S’88–M’91–SM’98) received the B.S. degree in electronic engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1983, the M.S. degree in electrical and computer engineering from Ohio University, Athens, in 1988, and the Ph.D. degree in electrical engineering and computer science from the University of Illinois, Chicago, in 1992.

From 1985 to 1986, he was a System Engineer in SAMPO, Inc., Taipei Hsien, Taiwan, where he was engaged in developing and designing graphic terminals. From 1988 to 1992, he was a Teaching and Research Assistant in the Department of Electrical Engineering and Computer Science (EECS), University of Illinois. Since 1993, he has been with the Electrical Engineering Department, National Chung Cheng University, Chia-Yi, Taiwan, where he is currently a Professor, and the Director of the Elegant Power Application Research Center (EPARC). His current research interests include developing and modeling of power converters, design of electronic dimming ballasts for fluorescent lamps, metal halide lamps and plasma display panels, design of solar array supplied inverters for grid connection, and design of pulsed-electrical-field generators for transdermal drug delivery and food pasteurization.

Dr. Wu is the recipient of three Best Paper Awards from Taipei Power Electronics Association during 2003–2005. In 2005, he was rated as one of the top 5% outstanding researchers by the National Science Council, Taiwan. He is a Senior Member of the International Commission on Illumination (CIE).

Jin-Chyuan Hung (S'99–M'05) received the B.S. degree in biomedical engineering from Chung Yuan Christian University, Chung-Li, Taiwan, R.O.C., in 1989, and the M.S. and Ph.D. degrees in electrical engineering from the National Chung Cheng University, Chia-Yi, Taiwan, in 1996 and 2005, respectively.

From 1996 to 1999, he was an Electrical Engineer at the Industry Technology Research Institute (ITRI), Hsin-Chu, Taiwan, where he was engaged in developing and designing high-voltage power supplies for X-ray generators, and where, from 2000 to 2002, he was a Design Engineer, developing hybrid electric vehicles (EVs). From 2005 to 2006, he was an R&D Manager at Delta Optoelectronics, Inc., Hsin-Chu, Taiwan, where he was involved in developing and designing driving systems of mercury-free flat fluorescent lamp (FFL) for liquid-crystal display (LCD) backlight applications. In 2006, he joined NuLight Technology Corporation, Tainan, Taiwan, where he is currently a Vice Division Director. His current research interests include development of soft-switching converters, design of the driving system of dielectric barrier discharge (DBD) lamps, and design of converters for EVs.

Jeng-Tsuen Tsai was born in Hsinchu, Taiwan, R.O.C., in 1980. He received the B.S. degree from the National Formosa University, Yunlin, Taiwan, in 2003, and the M.S. degree from the National Chung Cheng University, Chia-Yi, Taiwan, in 2005, all in electrical engineering.

In 2006, he joined NuLight Technology Corporation, Tainan, Taiwan, as a Senior Engineer. His current research interests include developing and designing of converter topologies, power-factor correctors, and flat-fluorescent lamp drivers.

Cheng-Tao Tsai was born in Taiwan, R.O.C., in 1962. He received the B.S. degree in electrical engineering from Feng Chia University, Taichung, Taiwan, in 1991, and the M.S. degree in electrical engineering in 2003 from the National Chung Cheng University, Chia-Yi, Taiwan, where he is currently working toward the Ph.D. degree in the Department of Electrical Engineering.

His current research interests include design of switching-mode power supplies, power factor correction technology, and chargers for electric vehicle.

Yaow-Ming Chen (S'96–M'98–SM'05) received the B.S. degree from the National Cheng-Kung University, Tainan, Taiwan, R.O.C., in 1989, and the M.S. and Ph.D. degrees from the University of Missouri, Columbia, in 1993 and 1997, respectively, all in electrical engineering.

From 1997 to 2000, he was with I-Shou University, Kaohsiung, Taiwan, as an Assistant Professor. In 2000, he joined the National Chung Cheng University, Chia-Yi, Taiwan, where he is currently an Associate Professor in the Department of Electrical Engineering. His current research interests include power electronic converters, power system harmonics and compensation, and intelligent control.