行政院國家科學委員會專題研究計畫 成果報告

應用於多輸入多輸出偵測系統之 K-Best 球型解碼演算法實現
研究成果報告(精簡版)

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計 畫 主 持 人：林光浩
共 同 主 持 人：曾振東
計畫參與人員：碩士班研究生-兼任助理人員：林孟毅
碩士班研究生-兼任助理人員：陳福期
碩士班研究生-兼任助理人員：陳柏軒
大專生-兼任助理人員：高堉雅

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中 華 民 國 100 年 08 月 30 日

行政院國家科學委員會補助專題研究計畫 ■成果報告 □期中進度報告

應用於多輸入多輸出偵測系統之 K-Best 球型解碼演算法實現

計畫類別：■個別型計畫　□整合型計畫
計畫編號：NSC　99－2221－E－167－033
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計畫主持人：林光浩
共同主持人：曾振東
計畫參與人員：林孟毅、陳福期、陳柏軒、高堉雅

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

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中　華　民　國　100 年　8 月　30　日

目　錄

行政院國家科學委員會專題研究計畫成果報告

應用於多輸入多輸出偵測系統之 K-Best 球型解碼演算法實現

A High-Throughput Modified Merge Sorting for MIMO Detection Systems

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主持人:林光浩 國立勤益科技大學電電子工程系
Email: khlin@ncut.edu.tw

摘要—MIMO 偵測器的功用主要是在接收端將收到的訊號，回復為原始的傳送端之 symbol。最大相似度偵測法是公認最佳化的演算法，有著最好的偵測效能，但運算複雜度將會隨著調變群集和傳送天線數目大小而呈指數型增加。因此 K-Best 球型解碼演算法就被提出來，他可以得到近似最大相似度偵測法的結果，並解決運算複雜度過多的問題。K-Best 球型解碼演算法在計算完部份歐幾里德距離後，需要取最小 K 個值做為候選點，在往下層去找候選點。因此需先將部份歐幾里德距離的結果做排序，再取出最小 K 個值。選取越多的 K 參數值，就越趨近最大相似度的偵測效能，但等待排序的資料量會變很大。因此本專題將針對 MIMO 偵測器的排序系統進行比較和改良，並改良出一個硬體體積小且速度快的排序電路，結合 bitonic merge 排序與奇偶排序提升其吞吐量與硬體效益。
關鍵詞: 多輸入多輸出，偵測器，排序。

Abstract—This paper proposed a high-throughput modified merge sorting for multiple-input multiple-output (MIMO) detection systems. The maximum likelihood detection (MLD) is an optimal detection method for MIMO communication systems, which is challenged by high computational complex-ity. Consequently, K-best decoding algorithm guarantees a fixed throughput and reduces the computational complexity. In order to achieve high throughput performances, the *K* candidates need to be fast sorting. This work presented the modified merge sorting which has combined the bitonic merge sorting with the odd-even merge sorting. By using the synthesis tool to analyze hardware structure, we can finally find out that the proposed modified merge sorting has high throughput and the best hardware efficiency.
Key Word: MIMO, Detector, Sorting.

I. INTRODUCTION

Multiple-input multiple-output (MIMO) systems have interested considerable research attentions in the wireless communication field. Recently, there have been many studies on practical techniques to realize the high channel capacity in MIMO systems. It has been shown in [1],[2] that high data rate wireless communication near *Gb/s* can be achieved in wireless local area networks (WLANs). The main challenge of the receiver design for MIMO systems lies in the detection of disorderly constellation. The MIMO techniques can basically be classified into space time coding (STC) and space division multiplexing (SDM) groups. STC increases the channel capacity of the wireless communication system by coding over different transmitter channels [3], whereas SDM employs multiple transmit and receive antennas and simultaneously transmits parallel data streams over all available spatial channels [4]. Especially, the high throughput technology has been discussed in SDM systems.

MIMO detector receives the signal and recovers it to the original transmitted symbol. Maximum likelihood detector (MLD) is the optimal detector and has the best performance. The challenge of MLD is the high computational complexity. K-Best decoding algorithm has been proposed to reduce the computational complexity [5]. K-Best decoder algorithm computes Partial Euclidean Distance (PED) and only keeps the best K nodes that have the smallest accumulated PEDs. After completing breadth-first tree search, we will have K leaves with the smallest PEDs. Therefore, K-Best algorithm is to find the K smallest PEDs and require an efficient sorting algorithm.

An improved sorting algorithm for K-Best MIMO detector is designed in this work. The sorter is based on the merge sorting and is much faster than the commonly used bubble sorting. The merge sort includes bitonic merge sorting and odd-even merge sorting. Owing to the better regularity structure of bitonic merge sorting [6] and the better hardware area efficiency of odd-even merge sorting [7], this work has proposed the modified merge sorting which has combined the bitonic merge sorting with the odd-even merge sorting.

This paper is organized as follows. Section II describes the MIMO detection including system model. Sorting architectures design are given in Section III. Section IV shows simulation results, and Section V concludes the paper.

II. MIMO DETECTION

A. MIMO System Model

To increase the data rate of the wireless communication, the spatial multiplex is used in the MIMO system with *Nt*

transmitted antennas and *Nr* received antennas. The baseband equivalent model can be described in Eq. (1).

$$\mathbf{Y=HS+n} \tag{1}$$

At each symbol time, a vector $\mathbf{S}=[s_1,s_2,..,s_{Nt}]^T$ with each symbol belonging to the *q* quadrature amplitude modulation (*q*-QAM) constellation passes through the channel response $Nr \times Nt$ matrix **H**. The received vector $\mathbf{Y}=[y_1,y_2,..,y_{Nr}]^T$ at the receiving antenna for each symbol time is a noisy superimposition of the *Nt* signals contaminated by additive white Gaussian noise (AWGN).

The complex matrix Eq. (1) can be transformed to its real matrix representation as Eq. (2).

$$\begin{bmatrix}\Re(\mathsf{Y})\\ \Im(\mathsf{Y})\end{bmatrix}=\begin{bmatrix}\Re(\mathsf{H}) & -\Im(\mathsf{H})\\ \Im(\mathsf{H}) & \Re(\mathsf{H})\end{bmatrix}\begin{bmatrix}\Re(\mathsf{S})\\ \Im(\mathsf{S})\end{bmatrix}+\begin{bmatrix}\Re(\mathsf{n})\\ \Im(\mathsf{n})\end{bmatrix} \tag{2}$$

B. K-Best Sphere Decoding Algorithm

The ML detector is the optimum detection algorithm for the MIMO system. It requires finding the signal point **S** from all transmit vector signal set that minimizes the Euclidean distance with respect to the received signal vector **y** with QR-decompositions as given in Eq. (3) ：

$$\hat{s}=\arg min\left\|\mathbf{Y}\text{-}HS\right\|^2=\arg min\left\|\hat{\mathbf{y}}\text{-}RS\right\|^2 \tag{3}$$

Expanding the vector norm in Eq. (3) yields into Eq. (4) ：

$$\hat{s}=\arg min\sum_{i=1}^{Nt}\left\|\hat{y}_i-R_{ii}S_i-\sum_{j=i+1}^{Nt}R_{ij}S_j\right\|^2 \tag{4}$$

The detection process starts from the last layers *l=Nt* and works the way until the first layer is detected. It is to perform an exhaustive search of all possible combinations of the transmitted symbols that minimizes $\left\|\mathbf{Y\text{-}HS}\right\|^2$.

The branch cost function associated with nodes in the *i*-th layer is：

$$T_i\left(s^i\right)=T_{(i+1)}\left(s^{(i+1)}\right)+\left|e_i\left(s^i\right)\right|^2$$

with $$e_i\left(s^i\right)=\hat{y}_i-R_{ii}S_i-\sum_{j=i+1}^{Nt}R_{ij}S_i \tag{5}$$

Each node in the tree corresponds to a so-called partial Euclidean distance （PED）$T_i(s^{(i)})$,where $T_{Nt+1}(s^{(Nt+1)})=0$ and term $|e_i(s^{(i)})|^2$ denotes the distance increment between two successive nodes in the tree.

At each layer, K-best detector approximates a breadth-first search by keeping only *K* candidates with the smallest PEDs are kept for the next level search. Therefore, at least K values need to be implemented with circuits. To meet the requirement of K-best detector system, a more popular sorting architecture, including bubble sorting, bitonic merge sorting and odd-even sorting, has been proposed, the modified merge sorting which can achieve fast sorting.

III. SORTING ARCHITECTURES

A. Bubble Sorting

Bubble sorting is the most common sorting technique, as shown in Figure 1. If there are *n* data ($I_1,I_2,\ldots I_n$) waiting for sorting, on the *1*st, *2*nd, …*n*th position, the first and the second data (I_1,I_2) will compare themselves with each other. The smaller results will be pushed down and the larger results will be pulled up. Similarly, comparing the second and the third data, pushing the smaller results down and pulling the larger ones up and so on. The minimum value can then be obtained from the first loop and the second minimum value from the second loop. Only eight minimum values are required in this work. After obtaining the eight minimum values from eight loops, sorting will be finished.

Therefore, when there are *n* data waiting for sorting, (n-1) loops will be needed. The first loop will give out the first maximum value by comparing (n-1) times while the second loop will give out the second maximum value by comparing (n-2) times. The time complexity will be $\mathbf{O}(n^2)$. Figure 1 deduces that we need n(n-1)/2 comparisons.

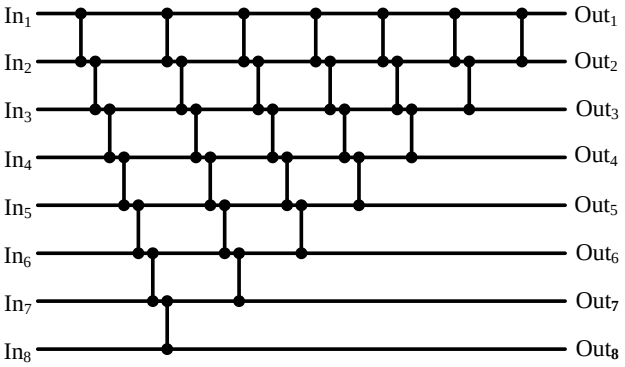

Figure 1. Diagram of bubble sorting.

B. Parallel Bubble Sorting

We can notice from the previous section that the sorting time and the waiting time of bubble sorting are in proportional relationships. In order to save time, comparison of I_3 and I_4 of the first loop and comparison of $I_1$and I_2 of the second loop will be carried out simultaneously. Therefore, at the same unit time, there will be different data processing, as shown in Figure 2. This method is called parallel bubble sorting whose time complexity is **O**(2n-3), requiring n(n-1)/2 comparisons.

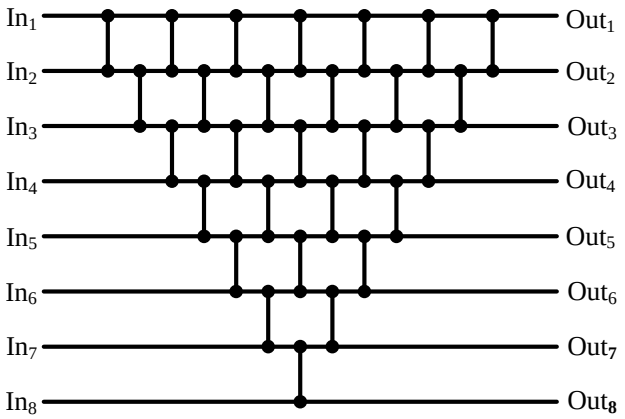

Figure 2. Diagram of parallel bubble sorting.

C. *Bitonic Merge Sorting*

Bitonic merge sorting means using two sorted sub-sequence for merging and sorting. For any sequence, we first divide the waiting data into groups of two, which we call Bi2. Then we merge pairs of Bi2 into four-input-four-output Bi4s. The output sequence (Out_1~Out_8) values are arranged from large to small.

For a *n*-input bitonic sorter, when it sets a bitonic sorting network, it forms a sequence according to Bi2,Bi4,…,Bi(n), as shown in Figure 3. Its time complexity is the sum of all the bitonic comparison orders, **O**($(\log_2 n(\log_2 n+1))/2$). Figure 3 deduces the number of comparisons required which is :

$$F_B(n)=\frac{n}{4}\log_2 n(\log_2 n+1) \qquad (6)$$

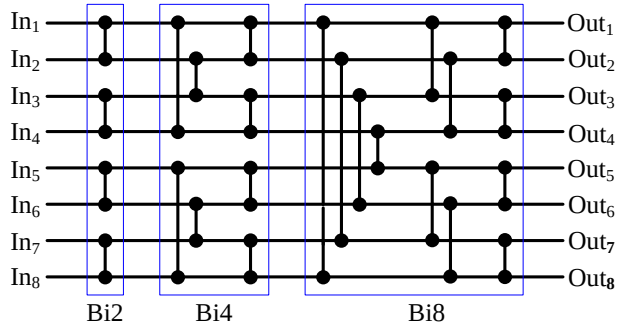

Figure 3. Diagram of bitonic sorting.

D. *Odd-Even Merge Sorting*

Odd-Even merge sorting is another merge sorting suggested by Batcher [7]. Different from bitonic sorting, odd-Even merge sorting uses two arranged sequence(A_1~A_4 and B_1~B_4) to merge sort odd numbers and even numbers respectively, as shown in Figure 4.

However, our input values need to be random numbers. Therefore, division must be done first, for any sequence, like bitonic. Divide the waiting data into groups of two, which we call Oe2, and then merge pairs of Oe2 into four-input-four-output Oe4s until the sorting is finished. Its time complexity is the same as bitonic merge sorting, **O**($(\log_2 n(\log_2 n+1))/2$), and comparisons are :

$$F_O(n)=2F(\frac{n}{2})+T(n) \qquad (7)$$

where $T(n)=\left(n(\log_2 n-1)/2\right)+1$ and $F(1)=0$.

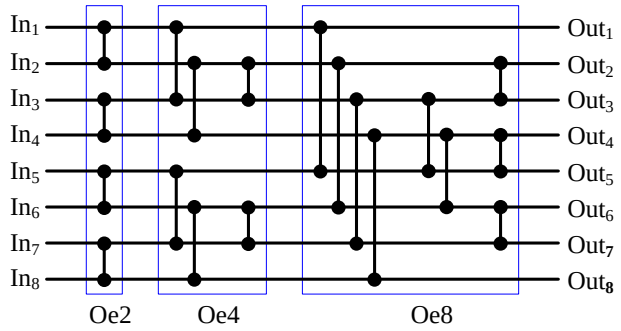

Figure 4. Diagram of odd-Even merge sorting.

E. *Modified Merge Sorting*

The requirement in this paper is 64 inputs but 8 minimum outputs. To prevent from finishing the whole sorting, this paper has make some improvements, making bitonic sorting better regularity and odd-even sorting better hardware area efficiency. Taking the advantages above, the time complexity is **O**($(\log_2 n(\log_2 n+1))/2$), with the least number of comparisons. When $n>8$, the required comparisons will be :

$$F_M(n)=2F_M(\frac{n}{2})+20 \qquad (8)$$

when $n\le 8$, the number of required comparisons will be the same as the odd-even merge sorting.

According to Table I and Table II, bubble sorting needs less comparisons but longer periods; parallel sorting requires less periods but still not fast enough, for K-best detector system needs high speed sorting circuit. From Table I, the periods of bitonic merge sorting, odd-even merge sorting and modified merge sorting are the same fast, but the hardware area efficiency in modified merge sorting is the best, with the least comparisons for sorting.

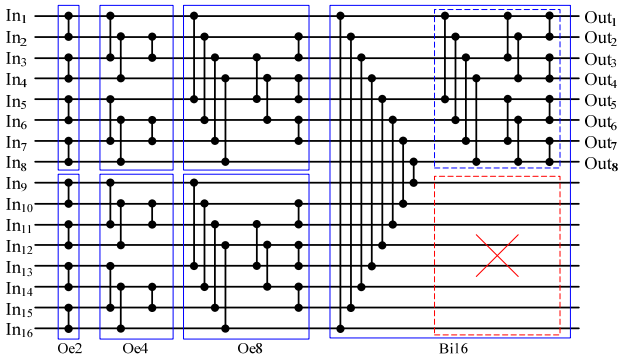

Figure 5. Diagram of modified merge sorting.

TABLE I. COMPARISONS OF TIME COMPLEXITY

Sorting Type	**Input Data (*n*)**		
	16	**32**	**64**
Bubble sorting (**O**)	256	1024	4096
Parallel bubble sorting (**O**)	29	61	125
Bitonic merge sorting (**O**)	10	15	21
Odd-Even merge sorting (**O**)	10	15	21
Modified merge sorting (**O**)	10	15	21

TABLE II. NUMBER OF REQUIRED COMPARATORS

Sorting Type	**Input Data (*n*)**		
	16	**32**	**64**
Bubble sorting	1	1	1
Parallel bubble sorting	8	16	32
Bitonic merge sorting	68	156	332
Odd-Even merge sorting	63	191	543
Modified merge sorting	58	136	292

IV. SIMULATION AND IMPLEMENTATION RESULTS

Most of the sorting circuits are basically composed of comparators. Figure 6(b) shows the defined comparator module, simplified in Figure 6(a). After comparing by the comparator, the Buffers will keep the data and the operating frequency can speed up, like the pipeline structure. Figure 7 is the proposed modified merge sorting structure. Like the pipeline structure, the 8 comparators can compare at the same time, therefore, fast sorting.

Figure 8 shows the simulation of the proposed modified merge sorting. Input 16 random values and then output 8 minimum values. Comparing all the sorting hardware data, as in Table 3, all kinds of sorting will have 64 inputs, containing 8-bit for each. By using the synthesis tool to analyze hardware structure, we can finally find out that the proposed modified merge sorting has high throughput and the best hardware efficiency. This paper has used ISE Xilinx device xc4vlx60-12ff1148 for FPGA hardware simulation and layout. The utility rate is shown as Table IV which also shows that the proposed utility rate suit the system best.

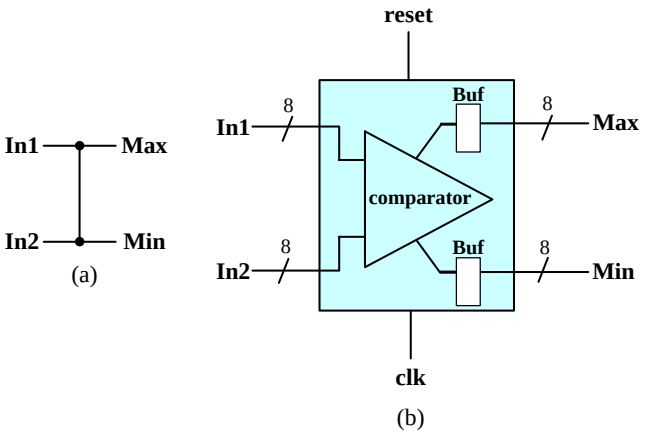

Figure 6. (a) Simplified comparator. (b) Comparator hardware structure.

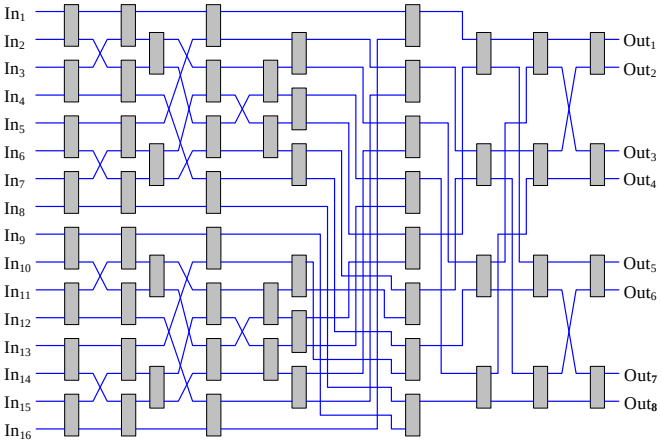

Figure 7. Hardware architecture of the Modified merge sort.

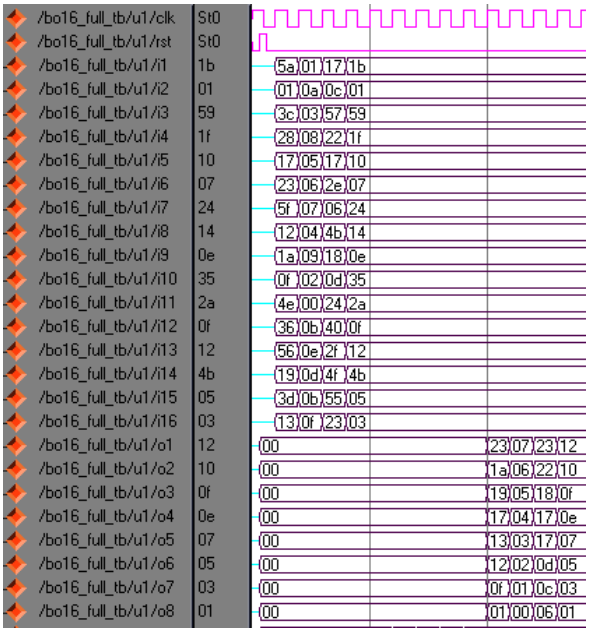

Figure 8. Simulation Result with the Modelsim.

TABLE III. ARCHITECTURE SYNTHESIS RESULTS

Sorting	Bubble	Parallel bubble	Bitonic merge	Odd-Even merge	Modified merge
Area(mm^2)	0.080	0.049	0.348	0.331	0.306
Operation Frequency (MHz)	85	85	85	85	85
Throughput (Mbps)	0.166	5.44	680	680	680
Power (mW)	11.978	36.603	45.910	48.129	44.794

TABLE IV. DEVICE UTILIZATION RESULTS WITH XILINX FPFA

Sorting	Bubble	Parallel bubble	Bitonic merge	Odd-Even merge	Modified merge
Number of Slice	4%	3%	9%	9%	8%
Number of LUTs	71%	10%	14%	12%	12%

V. CONCLUSION

This paper has made analysis and structure design on the sorting network of MIMO K-best detector in wireless communication. It has proposed a sorting called modified merge sorting which has taken the advantages of the superior structure of bitonic merge sorting and the small hardware of odd-even merge sorting. The hardware of the proposed one is even smaller than the odd-even one. For the sake of MIMO detector, this paper has implemented a 64-input modified merge sorting structure. When the operating frequency is at 85MHz, throughput can reach 680Mbps.

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行政院國家科學委員會補助國內專家學者出席國際學術會議報告

99 年 12 月 12 日

附件三

報告人姓名	林光浩	服務機構及職稱	國立勤益科技大學電子工程系助理教授
會議時間 會議地點	2010/12/6 ~ 2010/12/9 吉隆坡，馬來西亞	本會核定補助文號	NSC 99-2221-E-167-033
會議名稱	（中文）第 11 屆電路與系統亞太國際研討會 （英文）2010 IEEE Asia Pacific Conference on Circuits and Systems		
發表論文題目	（中文）應用於多輸入多輸出正交分頻多工系統之頻率漂移與 IQ 不平衡補償之低功率架構 （英文）Low-Complexity Architecture of CFO and IQI Compensation in MIMO-OFDM Systems		

報告內容應包括下列各項：

一、 參加會議經過

第 11 屆電路與系統亞太國際研討會(2010 IEEE Asia Pacific Conference on Circuits and Systems)是一個多樣化的會議，只要與電路或是系統相關的領域都可來參加此會議並學習目前新的技術與理論，此會議所包含的領域相當廣泛如下所示：

- Analog Signal Processing
- Biomedical Engineering
- Blind Signal Processing
- Cellular Neural Networks and Array Computing
- Circuits and Systems for Communications
- Circuits and Systems Education and Outreach
- Computer-Aided Network Design
- Digital Signal Processing
- Life-Science Systems and Applications

- Multimedia Systems and Applications
- Nanoelectronics and Gigascale Systems
- Neural Systems and Applications
- Nonlinear Circuits and Systems
- Power Systems and Power Electronic Circuits
- Sensory Systems
- Visual Signal Processing and Communications
- Test Technology
- System-on-Chip (SOC)
- Packaging
- MEMS Systems

會議第一天為報到日，在會場領取論文集光碟與大會手冊等相關資料。

接下來幾天，大會每天皆有安排 Keynote Speech ，主題包括了

Speaker Information	Title
Randall Geiger Iowa State university	Conventional Wisdom – Benefits and Consequences of Annealing Understanding of Engineering Principles
Shoji Kawahito Shizuoka University	Column-Parallel A/D Converters for CMOS Imager Sensors
Ljiljana Trajkovic Simon Fraser University	Analysis Of Internet Topologies
Ramesh Harjani University of Minnesota	Fun with Injection Locking
David Skellern National ICT Australia (NICTA)	The Internet of Things and the New Systems of the World
Bin-Da Liu National Cheng Kung University	Biosensors for Renal Function and Cellular Immunity Detection
N R Narayana Murthy Infosys Technologies	From Hardware Power to Software Power – A layperson's views
Jordan Plofsky Altera Malaysia	The semiconductor industry – the challenges ahead and the emergence of a new business model to overcome the challenges in SOC development

Eric WP Chan Embedded and Communications Group (ECG) Malaysia	Rise of Embedding Computing
Mike Kawasaki Agilent Electronic Instruments Marketing Manager and Worldwide Education Program Manager	New Technologies and Their Measurement Challenges

第二天開始便是一連串的論文報告，連續三天的 Presentation，而此會議的 Technical Sessions 一共有 59 Sessions 每個場次有六或七個題目的 Presentation，本論文則被安排在 12 月 9 日 Technical Sessions 之 RM9-S8 RF CircuitsVI。

本論文主要針對多輸入多輸出正交分頻多工（MIMO-OFDM）之低功率頻率漂移與 IQ 不平衡補償架構進行設計與製作，為提高整個補償的速度與性能，本論文創新將頻率漂移與 IQ 不平衡補償結合於晶片中，以硬體完成整個補償電路之製作，本論文並針對頻率漂移與 IQ 不平衡補償電路作一完整的分析與設計，經量測結果證明此晶片可完成 MIMO-OFDM 系統之同步工作。

二、 與會心得

參加此次研討會感受到學術交流的盛況，不論從會場外或會場內那種學術氣息讓人感覺到十分莊嚴，會議開始第一天主要安排報到行程所以氣氛較輕鬆，而會議第二天以後就開始真正論文研討會的探討，在大廳到處可看到

每個演講者正在準備下一場的報告，而在演講廳內已經如火如荼的展開一系列的論文探討，聽了幾個場次的論文報告覺得國外研究做的相當出色，而且各個領域的研究都在此能看到，所以能讓我對其他研究有更近一步的啟發。

本論文報告就在會議的第四天，一早起來就再次準備要報告的內容，一直到下午才由我上台報告，在報告過程中還蠻順利，所以對於參加國際研討會也有更深的體會，本論文報告結束後心情就比較放鬆，所以接下來的會議行程也比較愉快的心情去參與。整個研討會會議結束後，也完成此次國際性學術交流的目的，也讓我對研究領域的擴展助益良多。

三、 建議

感謝國科會對國內學者補助參與國際研討會所需費用，希望未來能繼續支持國內學者補助參與國際研討會。

四、 攜回資料名稱及內容

參加此次研討會帶回2010 IEEE Asia Pacific Conference on Circuits and Systems (Proceedings CD 一片) ，內容包括了所有的會議論文。

本人出國參加此次國際會議獲得國科會之補助，獲益良多，在此致上最深忱的謝意。

五、 其他

在此附上 2010 IEEE Asia Pacific Conference on Circuits and Systems 研討會會場照片與開會議程表。

報到會場照片紀錄

研討會行程表

2010 IEEE Asia Pacific Conference on Circuits and Systems
Circuits and Systems Scaling to Nanotechnology
December 6 - 9, 2010 Kuala Lumpur, MALAYSIA

Program Schedule

Day 1: Monday, 6th December 2010

Time	Program	Venue
08:00 am – 08:30 am	Tutorial Registration	Lake Garden Foyer (Hilton Kuala Lumpur)
08:30 am – 12:30 pm	Tutorial - Saeid Nooshabadi, Korea	Sentral Ballroom A (Hilton Kuala Lumpur)
	Tutorial - Krishnendu Chakrabarty, USA	Sentral Ballroom B (Hilton Kuala Lumpur)
10:00 am – 10:15 pm	Tea Break	Lake Garden Foyer (Hilton Kuala Lumpur)
12:30 pm– 14:00 pm	Lunch	
14:00 pm – 17:30 pm	Tutorial - Fuminori Kobayashi, Japan	Sentral Ballroom A (Hilton Kuala Lumpur)
	Tutorial - Maciej Ogorzalek, Poland and Giovanni DeMichelli, Switzerland	Sentral Ballroom B (Hilton Kuala Lumpur)
15:00 pm – 15:15 pm	Tea Break	Lake Garden Foyer (Hilton Kuala Lumpur)
17:30 pm – 18:30 pm	Conference Registration	Lake Garden Foyer (Hilton Kuala Lumpur)
18:30 pm – 20:00 pm	Welcome Reception	Lake Garden Foyer (Hilton Kuala Lumpur)

Program Schedule

Day 2: Tuesday, 7th December 2010

Time	Program	Venue
08:00 am - 09:00 am	Registration	Lake Garden Foyer
09:00 am - 10:00 am	Inaugural Lecture	Ballroom A (Hilton Kuala Lumpur)
10:00 am - 10:30 am	Tea Break	Ballroom C (Hilton Kuala Lumpur)
10:30 am - 12:30 am	Keynote-David Skellern, Australia	Ball Room A (Hilton Kuala Lumpur)
	Keynote - Shoji Kawahito, Japan	
	Keynote - Ramesh Harjani, USA	
12:30 pm– 14:00 pm	Lunch	Ballroom B (Hilton Kuala Lumpur)
14:00 pm - 15:30pm	Analog Signal Processing I	Sentral Ballroom A (Hilton Kuala Lumpur)
	Biomedical circuits and systems I	Sentral Ballroom B (Hilton Kuala Lumpur)
	Test Technology I	Sentral Accord & Network Room (Hilton Kuala Lumpur)
	Circuits and Systems for Communications I	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Computer-Aided Network Design I	Ballroom A (Hilton Kuala Lumpur)
	Digital Signal Processing I	Sultan's 1 (Le Meridien Kuala Lumpur)
	Visual Signal Processing and Communications I	Sultan's 2 (Le Meridien Kuala Lumpur)

	Multimedia Systems and Applications I	Hang Tuah 1 & 2 (Le Meridien Kuala Lumpur)
	RF Circuits I	Grand Salon (Le Meridien Kuala Lumpur)
	ADC / DAC I	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)
15:30 pm - 16:00pm	Tea Break	Ballroom C (Hilton Kuala Lumpur)
16:00 pm - 17:30pm	Analog Signal Processing II	Sentral Ballroom A (Hilton Kuala Lumpur)
	Biomedical circuits and systems II	Sentral Ballroom B (Hilton Kuala Lumpur)
	Test Technology II	Sentral Accord & Network Room (Hilton Kuala Lumpur)
	Circuits and Systems for Communications II	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Computer-Aided Network Design II	Ballroom A (Hilton Kuala Lumpur)
	Digital Signal Processing II	Sultan's 1 (Le Meridien Kuala Lumpur)
	Visual Signal Processing and Communications II	Sultan's 2 (Le Meridien Kuala Lumpur)
	RF Circuits II	Grand Salon (Le Meridien Kuala Lumpur)
	ADC / DAC II	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)
20:00 pm - 22:30pm	APCCAS2010 Banquet Dinner	Ballroom (Hilton Kuala Lumpur)

Program Schedule

DAY 3: Wednesday, 8th December 2010

Time	Program	Venue
08:30 am -10:30 am	Keynote - Ljiljana Trakovic, Canada	Ballroom A (Hilton Kuala Lumpur)
	Keynote - Randall Geiger, USA	
	Keynote - Agilent, Malaysia	
	Keynote - Bin-Da Liu, Taiwan	
10:30 am - 11:00am	Tea Break	Ballroom C (Hilton Kuala Lumpur)
11:00 am - 12:30pm	Special session: Advance Video Coding Algorithms and Architecture	Sentral Ballroom A (Hilton Kuala Lumpur)
	Special session: Algorithm/Architecture Design for Communications	Sentral Ballroom B (Hilton Kuala Lumpur)
	Special session: Biomedical Circuits and System Applications	Sentral Accord & Network Room (Hilton Kuala Lumpur)
	Special session: Circuits and Systems in Power Management	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Special session: Circuits for Portable Medical Electronic Systems	Hang Tuah 2 (Le Meridien Kuala Lumpur)
	Special session: Communication SoCs	Sultan's 1 (Le Meridien Kuala Lumpur)
	Special session: Manufacturing, Design, and Applications for 3-D Integration	Sultan's 2 (Le Meridien Kuala Lumpur)
	Special session: Multimedia SoC/IP Design	Grand Salon (Le Meridien Kuala Lumpur)
12:30 pm - 14:00pm	Lunch	Ballroom B (Hilton Kuala Lumpur)
	Analog Signal Processing III	Sentral Ballroom A (Hilton Kuala Lumpur)
	Biomedical circuits and systems III	Sentral Ballroom B (Hilton Kuala Lumpur)

14:00 pm - 15:30pm	Neural Systems and Applications	Sentral Accord & Network Room (Hilton Kuala Lumpur)
	Circuits and Systems for Communications III	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Power Systems and Power Electronic Circuits I	Hang Tuah 2 (Le Meridien Kuala Lumpur)
	Digital Signal Processing III	Sultan's 1 (Le Meridien Kuala Lumpur)
	System-on-Chip (SoC) I	Sultan's 2 (Le Meridien Kuala Lumpur)
	Nonlinear Circuits and systems I	Hang Tuah 1 (Le Meridien Kuala Lumpur)
	RF Circuits III	Grand Salon (Le Meridien Kuala Lumpur)
	ADC / DAC III	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)
15:30 pm - 16:00pm	Tea Break	Ballroom C (Hilton Kuala Lumpur)
16:00 pm - 17:30pm	Analog Signal Processing IV	Sentral Ballroom A (Hilton Kuala Lumpur)
	Biomedical Circuits and Systems IV	Sentral Ballroom B (Hilton Kuala Lumpur)
	MEMS System	Sentral Accord & Network Room (Hilton Kuala Lumpur)
	Circuits and Systems for Communications IV	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Power Systems and Power Electronic Circuits II	Hang Tuah 2 (Le Meridien Kuala Lumpur)
	Digital Signal Processing IV	Sultan's 1 (Le Meridien Kuala Lumpur)
	System-on-Chip (SoC) II	Sultan's 2 (Le Meridien Kuala Lumpur)
	Nonlinear Circuits and systems II	Hang Tuah 1 (Le Meridien Kuala Lumpur)
	RF Circuits IV	Grand Salon (Le Meridien Kuala Lumpur)
	Nano and Giga Scale System I	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)
18:30 pm - 20:30 pm	Dinner	Sultan's Ballroom (Le Meridien Kuala Lumpur)

Program Schedule

Day 4: Thursday, 9th December 2010

Time	Program	Venue
08:30 am -10:00am	Keynote - N R Narayan Murthy, India	Ballroom A (Hilton Kuala Lumpur)
	Keynote - Jordan Polaski, Malaysia	
	Keynote - Eric WP Chan, Malaysia	
10:00 am - 10:30am	Tea Break	Ballroom C (Hilton Kuala Lumpur)
10:30 am - 12:30pm	Idustrial Talk (ALTERA)	Ballroom A (Hilton Kuala Lumpur)
12:30 pm– 14:00 pm	Lunch	Ballroom B (Hilton Kuala Lumpur)
14.00 pm - 15.30 pm	Analog Signal Processing V	Sentral Ballroom B (Hilton Kuala Lumpur)
	Sensory Systems I	Sentral Exchange A & B (Hilton Kuala Lumpur)
	Digital Signal Processing V	Sultan's 1 (Le Meridien Kuala Lumpur)
	System-on-Chip (SoC) III	Sultan's 2 (Le Meridien Kuala Lumpur)

	Nonlinear Circuits and systems III	Hang Tuah 1 & 2 (Le Meridien Kuala Lumpur)
	RF Circuits V	Grand Salon (Le Meridien Kuala Lumpur)
	Nano and Giga Scale System II	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)
15:30 pm - 16:00pm	Tea Break	Ballroom C (Hilton Kuala Lumpur)
16.00 pm - 17.30 pm	Sensory Systems II	Sentral Exchange A & B (Hilton Kuala Lumpur)
	System-on-Chip (SoC) IV	Sultan's 2 (Le Meridien Kuala Lumpur)
	RF Circuits VI	Grand Salon (Le Meridien Kuala Lumpur)
	Nano and Giga Scale System III	Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur)

報告行程表

17.20 pm - 17.40 pm	1569336951	Switching Performance Analysis in RF MEMS Capacitive Shunt Switches by Geometric Parameters Trade-offs
		Parvin Bahmanyar;Khalil Mafinezhad; Mostafa Bahmanyar
RM4-S4 Sentral Exchange A & B (Hilton Kuala Lumpur) Circuits and Systems for Communications III		
Session Chair: Dr. Yuexian Zou & Assoc. Prof. Ashis Kumar Mal		
14.00 pm - 14.15 pm	1569320533	Start-up Analysis for Differential Ring Oscillator with Even Number of Stages
		Hui Zhang; Hai-gang Yang; Fei Lu; Yuan-feng Wei; Jia Zhang
14.15 pm - 14.30 pm	1569325407	Designing Asymmetric 2.2 GHz RF Oscillator by Design of Experiments using Taguchi Methods
		Jai Narayan Tripathi; Jayanta Mukherjee; Prakash R Apte
14.30 pm - 14.45 pm	1569321007	PPTWO: Push-Pull cell based traveling wave oscillator
		Yi Xu; Shuming Chen
14.45 pm - 15.00 pm	1569336703	A 3-GHz, 22-ps/dec Dynamic Comparator using Negative Resistance Combined with Input Pair
		Bo-Wei Chen; Chia-Ming Tsai; Jen-Peng Wang
15.00 pm - 15.15 pm	1569335875	A Novel Hybrid Matched Filter Structure for IEEE 802.22 Standard
		Zhang Zhang; Qingqing Yang; Linkai Wang; Xiaofang Zhou
15.15 pm - 15.30 pm	1569320688	A Signal Permutation Method for Cyclic-Prefix-Free OFDM Channel Estimation
		Shih-Hao Fang; Ju-Ya Chen; Ming-Der Shieh; Jing-Shiun Lin
RM4-S5 Sentral Exchange A & B (Hilton Kuala Lumpur) Circuits and Systems for Communications IV		
Session Chair: Prof. Seiya Abe		
16.00 pm - 16.15 pm	1569335389	A fully digital modulator/demodulator for Power Line Communication (PLC)
		Ko-Chi Kuo; Jia-Wei Guo; Yu-Hao Ou
16.15 pm - 16.30 pm	1569327327	A High Conversion Gain, Low Noise Figure RF-CMOS Receiver Front-End IC for 2.4-GHz Applications
		Mahyar Nirouei; Soheil Ziabakhsh; Hosein Alavi-Rad; Saman Ziabakhsh
16.30 pm - 16.45 pm	1569336391	A High Linearity 6th-Order Active R-MOSFET-C Band-Pass Filter for Power-line Communication
		Di Zhu; Jiacheng Wang; Chaoli Zhong; Jie Tian; Yiming Tang; Peiyuan Wan; Pingfen Lin
16.45 pm - 17.00 pm	1569328604	High-Speed and Low Power Unified Dual-Field Multiplier in GF (P) and GF (2^m)
		Prabhat Chandra Shrivastava; Arvind Kumar; Rupesh Kumar; Sanjeev Rai
17.00 pm - 17.15 pm	1569328707	A Low-Power Sub-threshold CMOS Continuous-Time Active-Filter with Reduced In-Band Noise for WiMAX Applications
		Milad Ataei; Mohsen Tamaddon; Abumoslem Jannesari
17.15 pm - 17.30 pm	1569329857	Low Power 0.18µm CMOS Ultra Wideband Inductor-less LNA Design for UWB Receiver
		Ali Shirzad Nilsaz; Mohsen Khani Parashkoh; Hossain Ghavamy-zadeh; Zhuo Zou; Majid Baghaei-Nejad; Li-Rong Zheng
RM5-S4 Hang Tuah 2 (Le Meridien Kuala Lumpur) Power Systems and Power Electronic Circuits I		
Session Chair: Prof. Shingo Yoshizawa & Prof. Khondker Zakir Ahmed		
14.00 pm - 14.15 pm	1569356961	A High Efficiency Boost White LED Driver with an Integrated Schottky Diode
		Yuan-Ta Hsieh; Bin-Da Liu; Jian-Fu Wu; Chiao-Li Fang; Hann-Huei Tsai; Ying Zong Juang
14.15 pm - 14.30 pm	1569320789	A High Precision Low Dropout Regulator with Nested Feedback Loops
		Ron-Chi Kuo; Tung-Han Tsai; Yi-Jie Hsieh; Chua-Chin Wang
14.30 pm - 14.45 pm	1569339615	Optimization of Control Switch for Energy Harvest Circuit Using Electrostatic Charges
		Helder Florentino; Raimundo Freire; Caio Florentino
14.45 pm - 15.00 pm	1569320961	Design and Analysis of an Interleave Controlled Series Buck Converter with Low Load Current Ripple
		Cai-Yang Ko; Tsorng-Juu Liang; Kai-Huin Chen; Jiann-Fuh Chen
15.00 pm - 15.15 pm	1569336909	Impact of Capacitors' Leakage Current Dispersion and a Simple approach to Improve
		Muhammad Mohsiul Haque; M. J. Alam
15.15 pm - 15.30 pm	1569328233	A Simplified PV Model for Low Power MPPT Controller Design
		Hirak Patangia; Srinikhil Gourisetti; Afzal Siddiqui; Sachin Sharma
RM5-S5 Hang Tuah 2 (Le Meridien Kuala Lumpur) Power Systems and Power Electronic Circuits II		
Session Chair: Prof. Tsorng-Juu (Peter) Liang		
16.00 pm - 16.15 pm	1569328671	Allocation of Network MW Flows to Bilateral Transactions
		Mohamed Shaaban
16.15 pm - 16.30 pm	1569329316	Design of a Linearly Increasing Inrush Current Limit Circuit for DC-DC Boost Regulators
		Khondker Zakir Ahmed; Mohammad Shahidul Islam; Syed Mustafa Khelat Bari; Mohammad Riazur Rahman Mazumder; A. B. M Harun-ur Rashid

16.30 pm - 16.45 pm	1569329439	Linear Optimal Control for Switching Converter
		Ghulam Abbas; Nacer Abouchi; Gael Pillonnet
16.45 pm - 17.00 pm	1569336295	High-Speed Low-Power Bootstrapped Level Converter for Dual Supply Systems
		Sang-Keun Han; Kee Chan Park; Bai-Sun Kong; Young-Hyun Jun
17.00 pm - 17.15 pm	1569336427	Battery Aware Tasks Allocating Algorithm for Multi-battery operated System
		Peng Ouyang; Shouyi Yin; Leibo Liu; Shaojun Wei
17.15 pm - 17.30 pm	1569335885	High Efficiency Power Management System for Solar Energy Harvesting Applications
		Ming-Hung Chang; Jung-Yi Wu; Shang-Yuan Lin; Wei-Chih Hsieh; You-Wei Liang; Wei Hwang
RM6-S4 Sultan's 1 (Le Meridien Kuala Lumpur) Digital Signal Processing III		
Session Chair: Prof. Youhua Shi		
14.00 pm - 14.20 pm	1569336109	An Efficient Quasi LMS/Newton Adaptive Algorithm for Stereophonic Acoustic Echo Cancellation
		Mehdi Bekrani; Mojtaba Lotfizad; Andy W. H. Khong
14.20 pm - 14.40 pm	1569336131	A Hardware-Efficient Color Segmentation Algorithm for Face Detection
		Kai-Ti Hu; Yu-Ting Pai; Shanq-Jang Ruan; Edwin Naroska
14.40 pm - 15.00 pm	1569336161	Perceptual Multiband Spectral Subtraction for Noise Reduction in Hearing Aids
		Cheng-Wen Wei; Shyh-Jye Jou; Cheng-Chun Tsai; Tian-Sheuan Chang
15.00 pm - 15.20 pm	1569336329	A New Regularized Transform-Domain NLMS Adaptive Filtering Algorithm
		Shing-Chow Chan; Yijing Chu; Zhiguo Zhang
15.20 pm - 15.40 pm	1569336457	Over Complementary MOS Logic for Don't Care Conditions
		Shun-Wen Cheng
RM6-S5 Sultan's 1 (Le Meridien Kuala Lumpur) Digital Signal Processing IV		
Session Chair: Prof. Jeich Mar		
16.00 pm - 16.20 pm	1569336601	Bangla Triphone HMM Based Word Recognition
		Mohammad Mahedi Hasan; Foyzul Hassan;Gazi Md. Moshfiqul Islam;Manoj Banik;Mohammed Rokibul Alam Kotwal; Sharif Mohammad Musfiqur Rahman; Ghulam Muhammad; Mohammad Huda
16.20 pm - 16.40 pm	1569336623	Optimal Register Assignment with Minimum-Delay Compensation for Latch-Based Design
		Keisuke Inoue; Kaneko Mineo
16.40 pm - 17.00 pm	1569336897	Quadratic Phase Coupling Analysis for Infrasound Vehicle Detection
		RenShi Li; Vinod Reddy; Andy W. H. Khong
17.00 pm - 17.20 pm	1569336975	Design and Implementation of Digital Image Processing Techniques in Pulse-Domain
		Fatemeh Taherian; Davud Asemani
17.20 pm - 17.40 pm	1569341001	Vehicle Tracking by Fusing Multiple Cues in Structured Environments Using Particle Filter
		Hamideh Rezaee; Ali Aghagolzadeh; Hadi Seyedarabi
RM7-S4 Sultan's 2 (Le Meridien Kuala Lumpur) System-on-Chip (SoC) I		
Session Chair: Prof. Haipeng Zhang		
14.00 pm - 14.15 pm	1569316079	An 8T SRAM Cell With Column-based Dynamic Supply Voltage for Bit-interleaving
		Tuan Do; Yeo Seng
14.15 pm - 14.30 pm	1569316531	Low IR Drop and Low Power Parallel CAM Design Using Gated Power Transistor Technique
		Tuan Do; Chen Shoushun
14.30 pm - 14.45 pm	1569320523	BusMesh NoC: A Novel NoC Architecture Comprised of Bus-based Connection and Global Mesh Routers
		Seungju Lee; Nozomu Togawa
14.45 pm - 15.00 pm	1569351491	Asynchronous Multi-Channel ADC and DSP Processor Interface
		Nennie Farina Mohat; Lam; Muhamad Khairol Ab Rani
15.00 pm - 15.15 pm	1569320043	Peeling Algorithm for Custom Instruction Identification
		Kang Zhao
15.15 pm - 15.30 pm	1569351451	On Power and Performance Tradeoff of L2 Cache Compression
		Tom Chen
RM7-S5 Sultan's 2 (Le Meridien Kuala Lumpur) System-on-Chip (SoC) II		
Session Chair: Dr. Nurul Amziah Md Yunus		
16.00 pm - 16.15 pm	1569320690	Efficient Protocol Converter Generation for System Integration
		Der-Wei Yang; Ming-Der Shieh; Wen-Hsuen Kuo; Jonas Wang
16.15 pm - 16.30 pm	1569325537	High-Performance 3D-SRAM Architecture Design
		Chun Lung Hsu; Ching-Fen Wu
16.30 pm - 16.45 pm	1569327479	A Mixed-Level Modeling for Network on Chip Infrastructure in SoC Design
		Yang Hu; Shouyi Yin; Leibo Liu; Shaojun Wei
16.45 pm - 17.00 pm	1569328123	A Configurable IP Core for Inverse Quantized Discrete Cosine and Integer Transforms with Arbitrary Accuracy

		Chi-Chia Sun; Ce Zhang Juergen Goetze
17.00 pm - 17.15 pm	1569328309	Star-Type Architecture with Low Transmission Latency for a 2D Mesh NOC
		Kuan-Ju Chen; Chin-Hung Peng; Feipei Lai
17.15 pm - 17.30 pm	1569337103	Panning Sorter: A Minimal-Size Architecture for Hardware Implementation of 2D Data Sorting Coprocessors
		Volnei Pedroni; Ricardo Jasinski; Ricardo Pedroni
RM8-S4 Hang Tuah 1 (Le Meridien Kuala Lumpur) Nonlinear Circuits and Systems I		
Session Chair: Professor Shiho Kim		
14.00 pm - 14.20 pm	1569319587	Current-Mode Multiphase Sinusoidal Oscillator Using Current-Controlled Current Differencing Transconductance Amplifiers
		Montree Kumngern
14.20 pm - 14.40 pm	1569319889	New Design for Output Power Improvement of a 20GHz Push-push FET DRO
		Sahar Bazar Ghadikolaei; Majid Tayarani
14.40 pm - 15.00 pm	1569328373	Area-Efficient Parallel-Prefix Ling Adders
		Tso-Bing Juang; Pramod Kumar Meher; Chung-Chun Kuan
15.00 pm - 15.20 pm	1569327653	A Sinusoidal Oscillator Using Translinear Current Conveyors
		Montree Kumngern; Somyot Junnapiya
15.20 pm - 15.40 pm	1569328163	Sensitivity Enhancement Using a Nonlinear Resonator
		Chenchen Deng; Steve Collins
RM8-S5 Hang Tuah 1 (Le Meridien Kuala Lumpur) Nonlinear Circuits and Systems II		
Session Chair: Assoc. Prof. Andy W. H. Khong		
16.00 pm - 16.15 pm	1569328551	Estimating Required Driver Strength in the Resonant Clock Generator
		Seyed Ebrahim Esmaeili; Asim Al-Khalili; Glenn Cowan
16.15 pm - 16.30 pm	1569329187	A Low Phase-Noise and Large Tuning Range 2.4GHz LC Voltage-Controlled Oscillator
		Siti Maisurah Mohd Hassan; Nazif Farid; Norman Fadhil Idham Muhammad; Ahmad Ismat Abdul Rahim; Mohamed Razman Yahya
16.30 pm - 16.45 pm	1569328221	Implementation of Low Power FFT Structure using a Method Based on Conditionally Coded Blocks
		Sandeep Saini; Anurag Mahajan; Srinivas B. Mandalika
16.45 pm - 17.00 pm	1569335571	Power and Jitter Optimized VCO Design Using an On-Chip Supply Noise Monitoring Circuit
		Yutao Liu; Ni Xu; Woogeun Rhee; Ziqiang Wang; Zhihua Wang
17.00 pm - 17.15 pm	1569335819	A Multiphase All-Digital Delay-Locked Loop with Reuse SAR
		Pao-Lung Chen; Tzu-Siang Wang; Jyun-Han Cou
17.15 pm - 17.30 pm	1569336883	A System-Level Non-linear Behavioral Modeling of Pulling and Pushing Mechanisms in PLLs
		Manohiaina Ranaivoniarivo; Sidina Wane; Elodie Richalot; Odile Picon
RM9-S4 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits III		
Session Chair: Prof. Haruichi Kanaya		
14.00 pm - 14.20 pm	1569328105	Current-Mode Echo Cancellation for Full-Duplex Chip-to-Chip Data Communication
		Vijaya Sankara Rao P; Pradip Mandal
14.20 pm - 14.40 pm	1569328138	Low-Cost Variable-Length FFT Processor for DVB-T/H Applications
		Jung Kisun; Hanho Lee
14.40 pm 15.00 pm	1569328703	Random Clock against Differential Power Analysis
		Kean Hong Boey; Yingxi Lu; Maire O'Neill; Roger Woods
15.00 pm - 15.20 pm	1569329193	Design and Analysis of Cost-Efficient IFFT/FFT Processor Chip for Wireless OFDM Systems
		Ting-Yuan Chen; Yi-Hsien Lin; Chih-Feng Wu; Chorng-Kuang Wang
RM9-S5 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits IV		
Session Chair: Assist. Prof. Anis Nurashikin Nordin		
16.00 pm - 16.20 pm	1569336402	Implementation of Topological Circuit Reduction
		Zdenek Kolka; Dalibor Biolek; Viera Biolkova; Martin Horak
16.20 pm - 16.40 pm	1569331709	Design and Evaluation of a 4x4 MIMO-OFDM Transceiver for Gigabit Indoor Wireless Communications
		Pei-Yun Tsai; Ze-Mu Chang; Zheng-Yu Huang; Wen-Ji Jau
16.40 pm - 17.00 pm	1569332041	A New Power Efficient Current-Mode 4-PAM Transmitter Interface for Off-Chip Interconnect
		Vijaya Sankara Rao P; Pradip Mandal
17.00 pm - 17.20 pm	1569337149	A Digital IF Based UHF RFID Reader Transmitter
		Zhang Chun; Lu Liang; Wang Jin Chao
17.20 pm - 17.40 pm	1569335955	A 40-GHz Phase-Locked Loop Front-End for 60-GHz Transceivers in 65nm CMOS
		Hammad Cheema; Reza Mahmoudi; Arthur van Roermund
RM10-S4 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) ADC / DAC III		

Session Chair: Prof. Saeid Nooshabadi		
14.00 pm - 14.20 pm	1569336071	An Energy-Efficient Successive Approximation Register Analog to Digital Converter in 180nm
		Taimur Gibran Kuntz; Saeid Nooshabadi
14.20 pm - 14.40 pm	1569329515	An FPGA Implemented 24-bit Audio DAC with 1-bit Sigma-Delta Modulator
		Xiaoxiao Li; Alex Lee
14.40 pm - 15.00 pm	1569319411	4-Bit Flash Analog to Digital Converter Design using CMOS-LTE Comparator
		Meghana Kulkarni; Sridhar V; Gururaj Kulkarni
15.00 pm - 15.20 pm	1569336463	A High Speed Tracking Quantizer for Continuous-Time Multi-Bit Sigma Delta Modulators
		Yoon Hwee Leow; Liter Siek
15.20 pm - 15.40 pm	1569336597	Analog-to-Digital Converter with Energy Recovery Capability Using Adiabatic Technique
		Howard Tang; Liter Siek
RM10-S5 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) Nano and Giga Scale System I		
Session Chair: Assoc. Prof. Dr. Sameh Ebrahim Rehan		
16.00 pm - 16.20 pm	1569321293	Effects of CNT Diameter Variability on a CNFET-Based SRAM
		Hamed Shahidipour; Yue Zhong; Arash Ahmadi; Koushik Maharatna
16.20 pm - 16.40 pm	1569328363	Efficient DFV-Aware Flip-Flops
		Chang Noh Yoon; Youngmin Cho; Jinsang Kim; Won-Kyung Cho
16.40 pm - 17.00 pm	1569328805	Design and characterisation of 16x1 parallel outputs SPAD array in 0.18 um CMOS technology
		Isaak Suhaila; Pitter Mark; Bull Steve; Harrison Ian
17.00 pm - 17.20 pm	1569329033	An ANN Majorty Logic Gate (MLG) Using Single Electron Nano-Devices
		Sameh Ebrahim Rehan
17.20 pm - 17.40 pm	1569329069	Continuous Wave (CW) sub-Terahertz (sub-THz) detection by Plasma Wave in High Electron Mobility Transistor (HEMT)
		Mohd Azlishah Othman; Harrison Ian

Oral Presentation Schedule		
DAY 4: Thursday, 9th December 2010		
RM2-S7 Sentral Ballroom B (Hilton Kuala Lumpur) Analog Signal Processing V		
Session Chair: Dr. Mohd Nizar Hamidon		
14.00 pm - 14.15 pm	1569328605	ADC Clock Jitter Measurement and Correction Using a Stochastic TDC
		Chi-Wei Fan; Jieh-Tsorng Wu
14.15 pm - 14.30 pm	1569335423	A Reduced Jitter-Sensitivity Clock Generation Technique for Continuous-Time ΣΔ Modulators
		Yang Jiang; Kim-Fai Wong; Chen-Yan Cai; Sin Weng; U Pan; Rui Martins
14.30 pm - 14.45 pm	1569336179	A 0.5V 65nm-CMOS Single Phase Clocked Bootstrapped Switch with Rise Time Accelerator
		Akira Shikata; Hiroki Ishikuro
14.45 pm - 15.00 pm	1569337087	A 0.5V 6-Bit Scalable Phase Interpolator
		Satoshi Kumaki; Hiroki Ishikuro
15.00 pm - 15.15 pm	1569320662	Elimination of Echoes From Voice Communication
		Mohd Zain Ismail; Abdul Halim Ali
15.15 pm - 15.30 pm	1569325505	Stochastic TDC Architecture with Self-Calibration
		Satoshi Ito; Shigeyuki Nishimura; Haruo Kobayashi; Satoshi Uemori; Yohei Tan; Nobukazu Takai; Takahiro Yamaguchi; Kiichi Niitsu
RM4-S7 Sentral Exchange A & B (Hilton Kuala Lumpur) Sensory Systems I		
Session Chair: Prof. Pei-Yun Tsai		
14.00 pm - 14.20 pm	1569316606	Environmental Taxonomy of Power Scavenging Techniques for Autonomous Self Powered Wireless Sensors
		Seyed Reza Kamel Tabbakh Farizani; Reyhaneh Maarefdoust; Chee Kyun Ng; Borhanuddin B Mohd. Ali
14. 20 pm - 14.40 pm	1569320943	Incremental Delta-Sigma A/D Converter for Ion-Sensitive System Application
		Bochau Lee; Wen-Yaw Chung; Mark Anthony Te
14.40 pm - 15.00 pm	1569325989	A Low-Power Switched-Capacitor Humidity Sensor Interface
		Pak Kwong Chan; Shuqin Ye
15.00 pm - 15.20 pm	1569328735	Travelling Route of Mobile Surveillance Camera
		Yoichi Tomioka; Atsushi Takara; Hitoshi Kitazawa
15.20 pm - 15.40 pm	1569329391	A Conductivity and Temperature Sensor Array for Detecting Saltwater Intrusion in Shore-Based Communities
		Marc Caesar Talampas; Paolo Angelo R. Fajardo; Rozelle C. Valdez; Michael Lochinvar S. Abundo
RM4-S8 Sentral Exchange A & B (Hilton Kuala Lumpur) Sensory Systems II		
Session Chair: Prof. Yue-Dar Jou		
16.00 pm - 16.20 pm	1569329927	Low-Noise Readout Circuits with a Response Time Acceleration Technique for High Output Impedance Sensors

		Mars Kamel; Shoji Kawahito
16.20 pm - 16.40 pm	1569330044	Clock-Gated and Low-Power Standard Cell Library for ISFET Two-Point Calibration Processor Chip
		Wen-Yaw Chung; Febus Reidj Cruz; Jian-Ping Chang
16.40 pm - 17.00 pm	1569339545	Automated Essay Content Analysis based on Concept Indexing with Fuzzy C-means Clustering
		Prospero C. Naval; Abigail R. Razon; Ma. Lourdes Vargas; Rowena Guevara
17.00 pm - 17.20 pm	1569336497	Footstep Detection and Denoising using a Single Triaxial Geophone
		Vinod Reddy; Divya Venkatraman; Andy W. H. Khong; Boon Poh Ng
17.20 pm - 17.40 pm	1569334415	Study on Coverage in Wireless Sensor Network using Grid Based Strategy and Particle Swarm Optimization
		Wan Zakiah Wan Ismail; S. Abd. Manaf
RM6-S7 Sultan's 1 (Le Meridien Kuala Lumpur) Digital Signal Processing V		
Session Chair: Dr. Harikrishnan A/L Ramiah		
14.00 pm - 14.15 pm	1569336747	Modeling of DLL-Based Frequency multiplier in TIme and Frequency Domain with Matlab Simulink
		Mohammad Gholami; Mohammad Sharifkhani; Saeed Saeedi
14.15 pm - 14.30 pm	1569336151	Systolic-Array 3D Wave-Digital Beam Filters
		Arjuna Madanayake; Leonard T. Bruton
14.30 pm - 14.45 pm	1569320081	A Simplified Approach for Baseband Recovery in SDR Architectures
		Richard Wee Tar Ng; Liter Siek
14.45 pm - 15.00 pm	1569329065	The Affine Transform and Feature Fusion for Robust Speaker Identification in the Presence of Speech Coding Distortion
		Robert Mudrowsky; Ravi Prakash Ramachandran; Sachin Shetty
15.00 pm - 15.15 pm	1569329527	Design of UWB Waveforms for Narrowband Interferences Suppression
		Mohd Amaluddin Yusoff; Zhuquan Zang
15.15 pm - 15.30 pm	1569327709	Weighted Least-Squares Design of IIR All-Pass Filters Using a Lyapunov Error Criterion
		Yue-Dar Jou; Fu-Kun Chen; Su Lo-Chyuan; Sun Chao-Ming
RM7-S7 Sultan's 2 (Le Meridien Kuala Lumpur) System-on-Chip (SoC) III		
Session Chair: Assoc. Prof. Dr. Roslina Mohd Sidek		
14.00 pm - 14.20 pm	1569329167	Routability-Driven Partitioning-Based IO Assignment for Flip-Chip Designs
		Jin-Tai Yan; Kai-Ping Lu; Zhi-Wei Chen
14.20 pm - 14.40 pm	1569329873	Design of Table-Based Function Evaluators with Reduced Memory Size Using a Bottom-Up Non-Uniform Segmentation Method
		Shen-Fu Hsiao; Chia-Sheng Wen; Kun-Chih Chen
14.40 pm - 15.00 pm	1569335735	A Fast Selector-Based Subtract-Multiplication Unit and Its Application to Radix-2 Butterfly Unit
		Youhei Tsukamoto; Masao Yanagisawa; Tatsuo Ohtsuki; Nozomu Togawa
15.00 pm - 15.20 pm	1569335943	Thermal-Aware Router-Sharing Architecture for 3D Network-on-Chip Design
		Yong-Ruei Huang; Jia-Hong Pan; Yi-Chang Lu
15.20 pm - 15.40 pm	1569336113	The Parallel Algorithm Implementation of Matrix Multiplication Based on ESCA
		Pan Chen; Kui Dai; Dan Wu; Jinli Rao; Xuecheng Zou
RM7-S8 Sultan's 2 (Le Meridien Kuala Lumpur) System-on-Chip (SoC) IV		
Session Chair: Dr. M. Iqbal Saripan		
16.00 pm - 16.15 pm	1569336333	Race Logic Synthesis for A Multithreaded HDL/ESL Simulator for soC Designs
		Terence Chan
16.15 pm - 16.30 pm	1569336421	A Low-latency GALS Interface Implementation
		Yuan-Teng Chang; Wei-Che Chen; Hung-Yue Tsai; Wei-Min Cheng; Chang-Jiu Chen; Fu-Chiung Cheng
16.30 pm - 16.45 pm	1569336537	Estimation-Based Run-Time Power Profile Flattening for RF-Powered Smart-Card Systems
		Andreas Genser; Christian Bachmann; Christian Steger; Reinhold Weiss; Josef Haid
16.45 pm - 17.00 pm	1569336581	B*-Tree based Variability-Aware Floorplanning
		Wenjuan Zhang; Shefali Srivastava; Yajun Ha
17.00 pm - 17.15 pm	1569336651	Efficient VLSI Architecture for Implementation of 1-D Discrete Wavelet Transform Based on Distributed Arithmetic
		Basant Kumar Mohanty; Anurag Mahajan
17.15 pm - 17.30 pm	1569337267	SEED Masking Implementations against Power Analysis Attacks
		Yingxi Lu; Kean Hong Boey; Maire O'Neill
RM8-S7 Hang Tuah 1 & 2 (Le Meridien Kuala Lumpur) Nonlinear Circuits and Systems III		
Session Chair: Prof. Dalibor Biolek		
14.00 pm - 14.15 pm	1569315505	Symbolic Analysis of the Tau Cell Log-Domain Filter
		Balavelan Thanigaivelan; Adam Postula; André van Schaik; Craig Jin; Tara Julia Hamilton
14.15 pm - 14.30 pm	1569319589	Electronically Tunable Multiple-Input Single-Output Voltage-Mode Multifunction Filter Employing Simple CMOS OTAs
		Montree Kumngem; Usa Torteanchai; Kobchai Dejhan
14.30 pm - 14.45 pm	1569321249	A 600MHz, 6th Order, Highly Linear Gm-C Bandpass Filter Design
		Saumen Mondal; Kumar Vaibhav Srivastava; Animesh Biswas
14.45 pm - 15.00 pm	1569336299	On Accuracy of Averaging for Switched Converters
		Zdenek Kolka; Dalibor Biolek; Viera Biolkova
15.00 pm - 15.15 pm	1569336611	Comparative Analysis of Switching Performance of Transistors in SOS process for RF Applications

		Robabeh Amirkhanzadeh; Henrik Sjoland; Ajay Tikka; Mike Faulkner
15.15 pm - 15.30 pm	1569350491	Effect of Impedance Variation around the Fundamentals on PA Distortions Characteristics under Wideband Multi-Tone Stimulus
		Shaiful Jahari Hashim; M. S. Hashmi; J. Benedikt; P. J. Taskar
RM9-S7 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits V		
Session Chair: Dr. Varun Jeoti		
14.00 pm - 14.20 pm	1569328279	Performance of MB-OWDM UWB Signals in Wireless Communications
		T. S. N. Murthy; K. Deergha Rao
14.20 pm - 14.40 pm	1569340721	A New ZCT Precoding Based SLM Technique for PAPR Reduction in OFDM Systems
		Imran Baig; Varun Jeoti
14.40 pm - 15.00 pm	1569336165	Space Vector PWM for PMSM Simulation using Matlab Simulink
		Anas Mohd Nazlee; Nor Hisham Hamid; Fawnizu Azmadi Hussin; Noohul Basheer Zain Ali
15.00 pm - 15.20 pm	1569340699	A New ZCT Precoded OFDM System with Pulse Shaping: PAPR Analysis
		Imran Baig; Varun Jeoti
15.20 pm - 15.40 pm	1569336349	Reconfigurable, Fast AFC Technique Using Code Estimation and Binary Search Algorithm for 0.2-6GHz Software-Defined Radio Frequency Synthesis
		Jun Li; Ni Xu; Yuanfeng Sun; Woogeun Rhee; Zhihua Wang
RM9-S8 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits VI		
Session Chair: Dr. Maryam Isa		
16.00 pm - 16.20 pm	1569336355	A Low-Power Radix-4 Viterbi Decoder Based on DCVSPG Pulsed Latch with Sharing Technique
		Xin-Ru Lee; Hsie-Chia Chang; Chen-Yi Lee
16.20 pm - 16.40 pm	1569336689	Baseband Receiver Design for 3GPP Long Term Evolution Downlink OFDMA Systems under Fast-Fading Channels
		Pei-Yun Tsai; Hsiang-Wei Chang; Po-Hsien Hsieh; Jhen-Yu Hou; Kang-Yi Fan
16.40 pm - 17.00 pm	1569336743	An efficient ODT calibration scheme for improved Signal integrity in memory interface.
		Kalyan Gudipati; M. B. Srinivas
17.00 pm - 17.20 pm	1569336981	Low-Complexity Architecture of CFO and IQI Compensation in MIMO-OFDM Systems
		Kuang-Hao Lin; Jan-Dong Tseng
RM10-S7 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) Nano and Giga Scale System II		
Session Chair: Dr Afandi Ahmad		
14.00 pm - 14.20 pm	1569329751	VLSI Implementation of a Fast Intra Prediction Algorithm for H.264/AVC Encoding
		Youhua Shi; Kenta Tokumitsu; Nozomu Togawa; Masao Yanagisawa; Tatsuo Ohtsuki
14.20 pm - 14.40 pm	1569352011	Interconnect Area, Delay and Area-Delay Optimization for Multi-level Signaling On-Chip Bus
		Fakhrul Zaman Rokhani; Mai Y. Ching; Ang T. Boon; Chin K. Yeong
14.40 pm - 15.00 pm	1569330801	Impact of HALO structure on Threshold Voltage and Leakage Current in 45nm NMOS Device
		Fauziyah Salehuddin; Ibrahim Ahmad; Azami Zaharim; Fazrena Hamid
15.00 pm - 15.20 pm	1569336203	A Cryogenic D/A Converter with Novel Charge Injection Reduction Technique for Silicon Quantum Computer Controller Circuit
		Md. Tanvir Rahman; Torsten Lehman
15.00 pm - 15.20 pm	1569336489	The Thermal-aware Floorplanning for 3D ICs using carbon nanotube
		Shengqing Shi; Xi Zhang; Rong Luo
RM10-S8 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) Nano and Giga Scale System III		
Session Chair: Dr. Fakhrul Zaman Rokhani		
16.00 pm - 16.20 pm	1569336519	A High Performance Vertical Si Nanowire CMOS for Ultra High Density Circuits
		Satish Maheswaran; Gaurav Kaushal; S. K. Manhas
16.20 pm - 16.40 pm	1569336563	Impact of Skew and Jitter on the Performance of VLSI Interconnects
		Gargi Khanna; Rajeevan Chandel; Ashwani Chandel
16.40 pm - 17.00 pm	1569339367	Negative ESD Robustness of a Novel Anti-ESD TGFPTD SOI LDMOS
		Haipeng Zhang; Liang Zhang; Dejun Wang; Guohua Liu; Mi Lin; Xiaoyan Niu; Lingyan Fan

Oral Presentation Schedule		
DAY 2: Tuesday, 7th December 2010		
RM1-S1 Sentral Ballroom A (Hilton Kuala Lumpur) Analog Signal Processing I		
Session Chair: Assoc. Prof. Changchuan Alex Lee		
14.00 pm - 14.20 pm	1569317431	Versatile High Input Impedance Voltage-Mode Three-Inputs Universal Biquadratic Filter
		Wei-Yuan Chiu, Jiun-Wei Horng, Zhao-Ren Wang
14.20pm - 14.40 pm	1569326681	A Tunable Transconductor With High Linearity
		Vijaya Bhadauria; Krishna Kant; Swapna Banerjee
14.40 pm - 15.00 pm	1569327805	An Unconditionally Stable Voltage Regulator
		Paulo Crepaldi; Tales C Pimenta; Robson Moreno; Edgar Rodriguez
15.00 pm - 15.20 pm	1569328773	A New Offset Cancelled Latch Comparator for High-Speed, Low-Power ADCs
		Khosrov Dabbagh Sadeghipour
15.20 pm - 15.40 pm	1569328963	Low Power Chopper Amplifier Without LPF
		Xiao Yang; Chaodong Ling
RM1-S2 Sentral Ballroom A (Hilton Kuala Lumpur) Analog Signal Processing II		
Session Chair: Dr. Jiun-Wei Horng & Prof. Shun-Wen Cheng		
16.00 pm - 16.15 pm	1569335625	Optimizing APT Product in MBFA Topologies
		Prashant Garg; Neeraj Chasta; Dipankar Nagchoudhuri
16.15pm - 16.30 pm	1569334807	High-Speed Low-Power Single-Stage Latched-Comparator with Improved Gain and Kickback Noise Rejection
		Sarang Kazeminia; Morteza Mousazadeh; Khayrollah Hadidi; Abdollah Khoei
16.30 pm - 16.45 pm	1569335671	A 25MHz Sign and Magnitude Converter for Analog Current Mode Iterative Decoders
		Ming Yam Lo; Wing-Hung Ki
16.45 pm - 17.00 pm	1569335687	Current-Mode Analog CMOS Fuzzy Logic Controller
		Mohammad Soleimani; Abdollah Khoei; Khayrollah Hadidi
17.00 pm - 17.15 pm	1569336087	A Highly Linear Open-Loop High-Speed CMOS Sample-and-Hold
		Morteza Mousazadeh; Khayrollah Hadidi; Abdollah Khoei
17.15 pm - 17.30 pm	1569337277	0.5 V Multi-Phase Digital Controlled Oscillator with Smooth Phase Transition Circuit
		Ahmad Tajudin Abul Hasan Johari; Hiroki Ishikuro
RM2-S1 Sentral Ballroom B (Hilton Kuala Lumpur) Biomedical Circuits and Systems I		
Session Chair: Assoc. Prof. Dr. Shanq-Jang Ruan		
14.00 pm - 14.20 pm	1569329007	FPGA-Based Architectures of Finite Radon Transform for Medical Image De-Noising
		Afandi Bin Ahmad; Abbes Amira; Hassan Rabah; Yves Berviller
14.20pm - 14.40 pm	1569328849	Design and Development of a Low Cost EMG Signal Acquisition System Using Surface EMG Electrode
		Tam Shi Poo; Kenneth Sundaraj
14.40 pm - 15.00 pm	1569320537	A Low-Power Remotely-Programmable MCU for Implantable Medical Devices
		Xiaoyu Zhang; Hanjun Jiang; Xinkai Chen; Chun Zhang; Zhihua Wang; Binjie ZHu
15.00 pm - 15.20 pm	1569329647	A Wireless Energy Link for Endoscopy with End-Fire Helix Emitter and Load-Adaptive Power Converter
		Tianjia Sun; Xie Xiang; Guolin Li; Yingke Gu; Xiaomeng Li; Zhihua Wang
15.20 pm - 15.40 pm	1569329847	A 77 nW Bioamplifier with a Tunable Bandwidth for Neural Recording Systems
		Iman Abaspur Kazerouni; Hadi Goodarzi Dehrizi; Sayed Mohammad Mostafavi Isfahani;
RM2-S2 Sentral Ballroom B (Hilton Kuala Lumpur) Biomedical Circuits and Systems II		
Session Chair: Prof. Yue-Dar Jou		
16.00 pm - 16.20 pm	1569329859	An Ultra-Low Power Multi-Tunable Triangle Wave Generator with Frequency and Amplitude Control
		Sayed Mohammad Mostafavi Isfahani; Iman Abaspur Kazerouni; Zhuo Zou; Majid Baghaei-Nejad; Li-Rong Zheng
16.20 pm - 16.40 pm	1569336633	Current Sensing Completion Detection for High Speed and Area Efficient Arithmetic
		Balapradeep Gadamsetti; Adit D Singh
16.40 pm - 17.00 pm	1569336279	Low-Noise Amplifier Path for Ultrasound System Applications
		Jayang Yoon; Jinseok Koh; Seok Lee; Jaehoon Kim; Namjin Song; Joongho Choi
17.00 pm - 17.20 pm	1569339337	CMRR Enhancement Technique for IA using Three IAs for Bio-medical Sensor Applications

		Woojae Lee; Min-Chang Cho; Seong Hwan Cho
17.20 pm - 17.40 pm	1569320521	Characterization of Endothelial Cells Using Electrochemical Impedance Spectroscopy
		Fei Liu; SM Arifuzzaman; Anis Nordin; David Spray; Ioana Voiculescu
RM3-S1 Sentral Accord & Network Room (Hilton Kuala Lumpur) Test Technology I		
Session Chair: Prof. G. Sobelman		
14.00 pm - 14.20 pm	1569315333	Combining Unspecified Test Data Bit Filling Methods and Run Length Based Codes to Estimate Compression, Power and Area overhead
		Usha Sandeep Mehta; K S Dasgupta; Niranjan Devashrayee
14.20pm - 14.40 pm	1569327697	ADC Linearity Test Signal Generation Algorithm
		Satoshi Uemori; Takahiro Yamaguchi; Satoshi Ito; Yohei Tan; Haruo Kobayashi; Nobukazu Takai; Kiichi Niitsu; N. Ishikawa
14.40 pm - 15.00 pm	1569327727	A Design Platform for Analog Device Size Sensitivity Analysis and Visualization
		Diming Ma; Guoyong Shi; Alex Lee
15.00 pm - 15.20 pm	1569328215	Jitter Generation and Capture using Phase-Domain Sigma-Delta Encoding
		Sadok Aouini; Kun Chuai; Gordon Roberts
15.20 pm - 15.40 pm	1569328623	Built-in Self-Test/Repair Scheme for TSV-Based Three-Dimensional Integrated Circuits
		Hung-Yen Huang; Yu-Sheng Huang; Chun Lung Hsu
RM3-S2 Accord Network Room (Hilton Kuala Lumpur) Test Technology II		
Session Chair: Prof. Ko-Chi Kuo		
16.00 pm - 16.20 pm	1569328889	Testing Techniques for Resistive-Open Defects in Future CMOS Technologies
		Mohammad Fawaz; Nader Kobrosli; Ali Chehab; Ayman Kayssi
16.20 pm - 16.40 pm	1569335663	A 9T Subthreshold SRAM Bitcell with Data-independent Bitline Leakage for Improved Bitline Swing and Variation Tolerance
		Qi Li; Tony Tae Hyoung Kim
16.40 pm - 17.00 pm	1569329621	RedSOCs-3D: Thermal-safe Test Scheduling for 3D-Stacked SoC
		Fawnizu Azmadi Hussin; Thomas Edison C Yu; Tomokazu Yoneda; Hideo Fujiwara
17.00 pm - 17.20 pm	1569336307	Non-Preemptive Test Scheduling for Network-on-Chip(NoC) Based Systems by Reusing NoC as TAM
		Goutam Mali; Suman Das; Hafizur Rahaman; Chandan Giri
RM4-S1 Sentral Exchange A & B (Hilton Kuala Lumpur) Circuits and Systems for Communications I		
Session Chair: Asst. Prof. Tony Tae Hyoung Kim		
14.00 pm - 14.15 pm	1569319283	A 4.8-Gb/s Mixed-mode CMOS QPSK Demodulator For 60-GHz Wireless Personal Area Networks
		Duho Kim; Minsu Ko; Kwang-Chun Choi; Woo-Young Choi
14.15pm - 14.30 pm	1569335665	Design of High Linearity Low Flicker Noise 5.2 GHz Down-Conversion Mixer for Direct Conversion Receiver
		Ramesh K Pokharel; Haruichi Kanaya; Youichi Yano; Mahmoud Ahmed Abdelghany; Keiji Yoshida
14.30 pm - 14.45 pm	1569336868	A Low Flicker Noise, Highly Linear, Direct Conversion Receiver for 5GHz Wireless LAN
		Mahmoud Ahmed Abdelghany; Haruichi Kanaya; Ramesh K Pokharel; Keiji Yoshida
14.45 pm - 15.00 pm	1569340791	An Electrically Small Meander Line Antenna for Wireless Applications
		Atif Jamil Shaikh; Mohd Zuki Yusoff; Noorhana Yahya
15.00 pm - 15.15 pm	1569320531	A 47-dB Linear CMOS Variable Gain Amplifier using Current Squaring Technique
		Xin Cheng; Hai-Gang Yang; Tongqiang Gao; Fei Liu
15.15 pm - 15.30 pm	1569333085	Introduction of a Pseudo-6th Order ISDN Splitter with Bandstop Topology
		Herbert De Pauw; Jan Doutreloigne; Andre Van Calster; Edmond Op de Beeck; Jurgen Content
RM4-S2 Sentral Exchange A & B (Hilton Kuala Lumpur) Circuits and Systems for Communications II		
Session Chair: Prof. Abigail Razon		
16.00 pm - 16.15 pm	1569325361	A 120dB All CMOS Variable Gain Amplifier Based on New Exponential Equation
		Farhad Sheikhhosseini; Abdolreza Nabavi
16.15pm - 16.30 pm	1569333783	The Transformer Coupled mm-Wave CMOS Power Amplifier
		Ki-Jin Kim; T. H. Lim; K. H. Ahn
16.30 pm - 16.45 pm	1569335509	A Concurrent Low-Area Dual Band 0.9/2.4 GHz LNA in 0.13µm RF CMOS Technology for Multi-Band Wireless Receiver
		Sambit Datta; Kunal Datta; Ashudeb Dutta; Tarun Kanti Bhattacharyya
16.45 pm - 17.00 pm	1569325267	Design and Simulation of a Lumped Element Metal Finger Capacitor for RF-CMOS Power Splitters
		Jasim Uddin; Anis Nordin; Muhammad IBN Ibrahimy; Mamun Bin Ibne Reaz

17.00 pm - 17.15 pm	1569328775	Transformer based front-end for a low power 2.4 GHz transceiver
		Jens Masuch; Manuel Delgado-Restituto; Ángel Rodríguez-Vázquez
17.15 pm - 17.30 pm	1569328985	Design and Analysis of the Current Reuse Technique and Folded Cascode Power Constrained Simultaneous Noise and Input Matching LNAs with distributed and lumped parasitic
		Norlaili Mohd. Noh; Awatif Hashim; Tan Kean Yeong; Tan Yong Yeap
RM5-S1 Ballroom A (Hilton Kuala Lumpur) Computer-Aided Network Design I		
Session Chair: Assoc. Prof. Pao-Lung Chen		
14.00 pm - 14.20 pm	1569327421	Design architecture of generic dft/dct 1d and 2d engine controlled by sw instructions
		Hanan M. Hassan; Ahmed F. Shalash; Hisham M. Hamed
14.20 pm - 14.40 pm	1569340749	An Overview of Vertical Handoff Decision Policies for Next Generation Wireless Networks
		Syed Safdar Ali Rizvi; Asif Aziz; Mohamad Naufal Mohamad Saad
14.40 pm - 15.00 pm	1569341123	A Comparative Analysis of Integration Schemes for UMTS and WLAN Networks
		Syed Safdar Ali Rizvi; Asif Aziz; Mohamad Naufal Mohamad Saad
15.00 pm - 15.20 pm	1569340902	Vehicle Tracking in Multi- Sensor Networks by Fusing Data in Particle Filter Framework
		Hamideh Rezaee; Ali Aghagolzadeh; M. Hadi Seyedarabi
RM5-S2 Ballroom A (Hilton Kuala Lumpur) Computer-Aided Network Design II		
Session Chair: Dr. Manuel Delgado-Restituto		
16.00 pm - 16.20 pm	1569328543	Controlled Placement and Routing Techniques to Improve Timing Balance of WDDL Designs in Mesh-Based FPGA
		Amouri Emna; Zied Marrakchi; Habib Mehrez
16.20 pm - 16.40 pm	1569328591	A SystemC Content Addressable Memory Power Estimation Tool for Early Design Verification
		I-Hui Tung; Kam-Tou Sio; Chin-Hung Peng; Lai Feipei
16.40 pm - 17.00 pm	1569328593	CAM Puzzle: A Power Model and Function-Based Circuit Segment Method of Content Addressable Memory
		Kam-Tou Sio; Lai Feipei; Chin-Hung Peng
17.00 pm - 17.20 pm	1569334977	On the optimization of FPGA area depending on target applications
		Zied Marrakchi; Hamied Marrakchi; Husain Parvez Alp Klic; Habib Mehrez
17.20 pm - 17.40 pm	1569337173	Achieving Near-MLD Performance with Soft Information-Set Decoders Implemented in FPGAs
		Antonio Gortan; Ricardo Jasinski; Walter Godoy Jr.; Volnei Pedroni
RM6-S1 Sultan's 1 (Le Meridien Kuala Lumpur) Digital Signal Processing I		
Session Chair: Prof. Usha Sandeep Mehta		
14.00 pm - 14.20 pm	1569324871	Multi-Stage Lattice-Reduction-Aided MIMO Detector Using Reverse-Order LLL algorithm
		Chun-Fun Liao; Li-Wei Chai; Po-Lin Chiu; Yuan-Hao Huang
14.20 pm - 14.40 pm	1569336765	Mitigation of GPS Multipath Error Using Recursive Least Squares Adaptive Filtering
		Yedukondalu K; A. D. Sarma; Ashwani Kumar
14.40 pm - 15.00 pm	1569328164	Computation Sharing Multiplier Using Redundant Binary Arithmetic
		R.S.N. Kumar Kattamuri; S.K. Sahoo
15.00 pm - 15.20 pm	1569328847	An All-Digital De-skew Clock Generator for Arbitrary Wide Range Delay
		Kevin Fong; Yu-Cheng Hung; Zuow-Zun Chen; Tai-Cheng Lee;
15.20 pm - 15.40 pm	1569335985	Fusion Methods for Boosting Performance of Speaker Identification Systems
		Gregory Ditzler; James Ethridge; Kavi Prakash Ramachandran; Robi Polikar
RM6-S2 Sultan's 1 (Le Meridien Kuala Lumpur) Digital Signal Processing II		
Session Chair: Prof. Dr. Ravi P. Ramachandran		
16.00 pm - 16.20 pm	1569331281	A High Speed and Low Power 4:1 Multiplexer with Cascoded Clock Control
		Jin-Hyung Park; Ji-Seop Song; Shin Il Lim; Suki Kim
16.20 pm - 16.40 pm	1569334447	A PCI166-compatible 3xVDD-Tolerant Mixed-Voltage I/O Buffer
		Ron-Chi Kuo; Hsiao-Han Hou; Chua-Chin Wang
16.40 pm - 17.00 pm	1569335391	Low Power Level Shifter and combined with Logic Gates
		Ko-Chi Kuo; Sheng-Quane Chen
17.00 pm - 17.20 pm	1569327719	Ambiguity Function of Non-Stationary Signals Using Wavelet Transform
		Reza Kayvan shokooh; Mohammad Alaee; Majid Okhovvat; Reza Amin
17.20 pm - 17.40 pm	1569328037	High Accuracy Binary Logarithmic Conversion using Range Mapping for DSP Applications
		Joshua Yung Lih Low; Low Ching Chuen Jong
RM7-S1 Sultan's 2 (Le Meridien Kuala Lumpur) Visual Signal Processing & Communications I		
Session Chair: Assoc. Prof. Dr. Abdul Halim bin Ali		
14.00 pm - 14.20 pm	1569321331	A Moving Vehicle Segmentation Method Based on Clustering of Feature Points for Tracking at Urban Intersection

		Yuexian Zou; He Zhao; Hang Shi; Yiyan Wang
14.20 pm - 14.40 pm	1569337665	A Dynamic Search Range Algorithm for H.264/AVC Full-Search Motion Estimation
		Yuan-Teng Chang; Wen-Hao Chung
14.40 pm - 15.00 pm	1569328030	A Subspace Approach for Restoring Image Corrupted by White Noise
		Norashikin Yahya; Nidal Kamel; Aamir S Malik
15.00 pm - 15.20 pm	1569329115	Optimal Discrete Wavelet Transform (DWT) Features for Face Recognition
		Afandi Bin Ahmad; Abbes Amira; Paul Nicholl
15.20 pm - 15.40 pm	1569335647	Motion Estimation based on Iterative Color Matching and Structure Matching
		Zhu Li; Yoichi Tomioka; Hitoshi Kitazawa
RM7-S2 Sultan's 2 (Le Meridien Kuala Lumpur) Visual Signal Processing & Communications II		
Session Chair: Dr. Danny Wen-Yaw Chung		
16.00 pm - 16.20 pm	1569336257	Complexity Reduction Algorithm for Region-of-Interest based H.264 Encoding
		Tianruo Zhang; Minghui Wang; Chen Liu; Satoshi Goto
16.20 pm - 16.40 pm	1569336339	Image-Based Compression, Prioritized Transmission and Progressive Rendering of Circular Light Fields (CLFS) For Ancient Chinese Artifacts
		X. Z. Yao; S. C. Chan; Z. Y. Zhu; K. T. Ng; H. Y. Sum
16.40 pm - 17.00 pm	1569336359	Gait Recognition using Occluded Data
		Wan Noorshahida Mohd-Isa; Md Jahangir Alam; Chikkanan Eswaran
17.00 pm - 17.20 pm	1569336607	Connected-Component Stereo Aggregation
		Ng Oon-Ee; Velappa Ganapathy; S. G. Ponnambalam
RM8-S1 Hang Tuah 1 & 2 (Le Meridien Kuala Lumpur) Multimedia Systems & Applications I		
Session Chair: Assoc. Prof. Shuenn-Yuh Lee & Dr Mohamed Abd El-Moneim Shaaban		
14.00 pm - 14.15 pm	1569336453	A novel predictor cofficient Interpolation Algorithm for enhancement of spatial resolution of images
		Vinit Jakhetiya; Sunil Prasad Jaiswal; Anil Kumar Tiwari
14.15pm - 14.30 pm	1569315289	A Fast and Low-Cost Fractional Motion Estimation for H.264/AVC HD1080p Coding
		Yuan-Teng Chang; Wen-Hao Chung
14.30 pm - 14.45 pm	1569321957	Nearly lossless optimization of 1/2 pixel interpolation for H.264 decoder
		Q Wang; He Yuwen
14.45 pm - 15.00 pm	1569336417	Human Tracking System for Automatic Video Surveillance with Particle Filters
		Joshua Yung Lih Low; Ching Chuen Jong
15.00 pm - 15.15 pm	1569329498	Building a Real-Time High Definition Multiple Video Streaming System based on Intel IPP H.264
		Vishnu Monn Baskaran; KokSheik Wong; Yeong Sheng Low
15.15 pm - 15.30 pm	1569335335	A Design of Bandwidth Adaptive Multimedia Gateway for Scalable Video Coding
		Yi-Mao Hsiao; Su-Wei Yeh; Jai-Shiarng Chen; Yuan-Sun Chu
15.30 pm - 15.45 pm	1569328154	Audio Mixer with Automatic Gain Controller for Software Based Multipoint Control Unit
		Vishnu Monn Baskaran; Kok Sheik Wong
RM9-S1 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits I		
Session Chair: Prof. Song Chen		
14.00 pm - 14.15 pm	1569318859	Design of an EEPROM in RFID Tag: Employing Mapped EPC and IPv6 Address
		Labonnah F Rahman; Mamun B.I Reaz; Mohd Alauddin Mohd Ali; Masaru Kamada
14.15 pm - 14.30 pm	1569328931	Design of Ultra Low Power Stream Data Receiver Based on UHF Passive RFID Tag System
		Seok Joong Hwang; Seon Wook Kim; Joon-goo Lee; Dong Ha Jung; Areum Kim
14.30 pm - 14.45 pm	1569331517	Development of Active RFID System Using ZigBee Standard with Non-Beacon Mode
		Mohd Aminuddin Shahimi; Z. Abdul Halim; W. Ismail
14.45 pm - 15.00 pm	1569335283	Drawing on the Benefits of RFID and Bluetooth Technologies
		Assim Sagahyroon; Mohammed Eqbal; Farshad Khamisi
15.00 pm - 15.15 pm	1569336459	A Novel 6.5 pJ/Pulse Impulse Radio Pulse Generator for RFID Tags
		Kin Keung Lee; Malihe Zarre Dooghabadi; Håkon A. Hjortland; Øivind Næss; Tor Sverre Lande
15.15 pm - 15.30 pm	1569329144	Design Issues and Optimization in DisplayPort Link Layer Implementation
		Jaegeun Oh; Seon Wook Kim; Taejin Kim
RM9-S2 Grand Salon (Le Meridien Kuala Lumpur) RF Circuits II		
Session Chair: Assist. Prof. Sanjeev Rai		
16.00 pm - 16.20 pm	1569320495	SDR Structure Based CFO Estimation and Compensation Circuit for OFDM Systems Using Reconfigurable CORDIC FPGA Modules

		Jeich Mar; Chi-Cheng Kuo; Shih-Hao Chou
16.20 pm - 16.40 pm	1569336977	A CMOS Synthesizer using a new scheme of injection locking of VCOs
		Hassan Sepehrian; Masoud Rezaei; Sasan Naseh
16.40 pm - 17.00 pm	1569321647	Ultrasonic and Infrared Repelling Device for Controlling the Population of Rat in Paddy Field
		Muhammad Assaqaf; Mohd Fisol; Warsuzarina Mat Jubadi
17.00 pm - 17.20 pm	1569325827	IQ Imbalance Compensation: A Semi-Blind Method for OFDM Systems in Fast Fading Channels
		Lan Lan He; Shaodan Ma; Yik-Chung Wu; Tungsang Ng
17.20 pm - 17.40 pm	1569340969	Channel Estimation and Detection for Multibeam Satellite Communications
		Helmi Chaouech; Ridha Bouallegue
RM10-S1 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) ADC / DAC I		
Session Chair: Prof. Shingo Yoshizawa		
14.00 pm - 14.20 pm	1569326131	A Precision Low-Power Mismatch-Compensated Sample-and-Hold Circuit for Biomedical Applications
		Sai Lei Mak; Pak Kwong Chan; Shiv Kumar Mishrae
14.20 pm - 14.40 pm	1569326283	Non-Binary SAR ADC with Digital Error Correction for Low Power Applications
		Tomohiko Ogawa; Tatsuji Matsuura; Haruo Kobayashi; Nobukazu Takai; Masao Hotta; Hao San; Akira Abe; Katsuyoshi Yagi; Toshihiko Mori
14.40 pm - 15.00 pm	1569327699	Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier Using Split ADC Structure
		Takuya Yagi; Kunihiko Usui; Tatsuji Matsuura; Satoshi Uemori; Yohei Tan; Satoshi Ito; Haruo Kobayashi
15.00 pm - 15.20 pm	1569328901	Low Power, Variable Resolution Pipelined Analog to Digital Converter with Sub Flash Architecture
		Adimulam Mahesh; Krishna Movva; Veeramachaneni Sreehari; Moorthy Muthukrishnan; MB Srinivas
15.20 pm - 15.40 pm	1569328929	An Efficient DAC and Interstage Gain Error Calibration Technique For Multi-Bit Pipelined ADCs
		Li Ding; Sai-Weng Sin; Seng-Pan U; Rui Martins
RM10-S2 Hang Jebat 1 & 2 (Le Meridien Kuala Lumpur) ADC / DAC II		
Session Chair: Prof. Khosrov Dabbagh Sadeghipour		
16.00 pm - 16.20 pm	1569331513	Development of Low Power DAC with Pseudo Fibonacci Sequence
		Ryota Kubokawa; Haruichi Kanaya; Takashi Ohshima
16.20 pm - 16.40 pm	1569334445	SAR ADC That is Configurable to Optimize Yield
		Tomohiko Ogawa; Haruo Kobayashi; Yohei Tan; Satoshi Ito ; Satoshi Uemori; Nobukazu Takai; Kiichi Niitsu; Takahiro Yamaguchi; Tatsuji Matsuura; N. Ishikawa
16.40 pm - 17.00 pm	1569336045	A 10-Bit 1.25GSample/s Partially-Segmented D/A Converter For Ultra Wide-Band Communication System
		Soon-Ik Cho; Shin-Il Lim; Suki Kim
17.00 pm - 17.20 pm	1569336184	A Fast Bootstrapped Switch for High-Speed High-Resolution A/D Converter
		Guanzhong Huang; Pingfen Lin
17.20 pm - 17.40 pm	1569336719	A Weighted Capacitor Digital-to-Analog Converter Adopting Extensive Charge Sharing Scheme.
		Taeho Lim; K. J. Kim; K. H. Ahn; J.S. Kim

Oral Presentation Schedule		
DAY 3: Wednesday, 8th December 2010		
RM1-S4 Sentral Ballroom A (Hilton Kuala Lumpur) Analog Sinal Processing III		
Session Chair: Assoc. Prof. Vijaya Bhadauria		
14.00 pm - 14.20 pm	1569327747	Design of DXT Architecture Using Current-Switched Integrator
		Ashis Kumar Mal; Rishi Todani; Anindya S. Dhar
14.20 pm - 14.40 pm	1569327749	A Low Voltage Current Mirror Based on Quasi-Floating Gate MOSFETs
		Susheel Sharma; Rockey Gupta; Sudhanshu S. Jamuar
14.40 pm - 15.00 pm	1569328737	Low Voltage Regulated Cascode Current Mirrors Suitable for Sub-1V Operation
		Prateek Vajpayee; Anurag Srivastava; Sher Rajput; Gopal Sharma
15.00 pm - 15.20 pm	1569329613	Post-Scheduling Frequency Assignment for Energy-Efficient High-Level Synthesis
		Ru Liu; Song Chen; Takeshi Yoshimura
15.20 pm - 15.40 pm	1569329478	Implementation of Highly Accurate NMOS Vt Based Clamping Technique in Low Current Comparator
		Mustafa Ryadh; Khondker Zakir Ahmed
RM1-S5 Sentral Ballroom A (Hilton Kuala Lumpur) Analog Sinal Processing IV		
Session Chair: Prof. Tyrone Fernando		
16.00 pm - 16.20 pm	1569335827	0.8-µW CMOS Bulk-Driven Linear Operational Transconductance Amplifier in 0.35-µm Technology

		Apiradee Yodtean
16.20 pm - 16.40 pm	1569326187	Fully-Differential Low-Offset Interface for Capacitive Sensors
		Kaimin Zhou; Zhihua Wang
16.40 pm - 17.00 pm	1569336023	A Temperature-Stabilized Voltage Reference Utilizing MOS Body Effect
		Haesick Sul; Young-Hyun Jun; Bai-Sun Kong
17.00 pm - 17.20 pm	1569339371	Numerical Implementation of a Functional Observability Algorithm: A Singular Value Decomposition Approach
		Tyrone Fernando; Les Jennings; Hieu Trinh
17.20 pm - 17.40 pm	1569336375	Mutators Simulating Memcapacitors and Meminductors
		Dalibor Biolek; Viera Biolkova; Zdenek Kolka
RM2-S4 Sentral Ballroom B (Hilton Kuala Lumpur) Biomedical Circuits and Systems III		
Session Chair: Dr. Hsin Chen		
14.00 pm - 14.20 pm	1569328211	Novel Hybrid Approach Combining ANN and MRA for PET Volume Segmentation
		Mhd Saeed Sharif; Maysam F Abbod; Abbes Amira; Habib Zaidi
14.20 pm - 14.40 pm	1569329925	Preamplifier Effect on the Performance of Distributed Active Mixer
		Zahra Zare; Ahmad Hakimi; Farhad Sheikhhosseini; Masoud Movahhedi
14.40 pm - 15.00 pm	1569334783	3D Multiresolution Analysis for Reduced Features Segmentation of Medical Volumes Using PCA
		Shadi AlZubi; Naveed Islam; Maysam F Abbod
15.00 pm - 15.20 pm	1569335393	Application of Gyroscopes in Identifying Gait Symmetry in Walking
		Darwin Gouwanda; Arosha SM Nanmal Senanayake
15.20 pm - 15.40 pm	1569336167	Smart Wearable Device for Real time Gait Event Detection during Running
		Aruni Alahakone; Arosha SM Nanmal Senanayake; Chathuri Senanayake
RM2-S5 Sentral Ballroom B (Hilton Kuala Lumpur) Biomedical Circuits and Systems IV		
Session Chair: Dr. Siti Anom Ahmad		
16.00 pm - 16.20 pm	1569327847	Effects of Exercise on the Second Derivative Photoplethysmography (PPG) Waveform
		Rusealiza Mohamad Rozi; Mohd Alauddin Mohd Ali; Mamun B.I Reaz
16.20 pm - 16.40 pm	1569329215	The Application of Ultrasonic Transducer in Bacteria Growth Monitoring System
		Aini Salwa Hasan Nudin; Kenneth Sundaraj; Azian Azamimi Abdullah; Muhamed Zulkali Muhamed Daud
16.40 pm - 17.00 pm	1569336713	Signal and Noise Separation in Medical Diagnostic System based on Independent Component Analysis
		Abdullah Khan; Kenji Hashiodani; Tatsuya Onoue; Yohei Fukumizu; Hironori Yamauchi
RM3-S4 Sentral Accord & Network Room (Hilton Kuala Lumpur) Neural Systems and Applications		
Session Chair: Prof. Majid Baghaei-Nejad		
14.00 pm - 14.20 pm	1569335895	A hybrid architecture for efficient FPGA-based implementation of multilayer neural network
		Zhen Lin; Yiping Dong; Yan Li; Takahiro Watanabe
14.20 pm - 14.40 pm	1569336846	A Modified Discrete Recurrent Neural Network as Vector Detector
		Mohamad Mostafa; Werner G. Teich; Juergen Lindner
14.40 pm - 15.00 pm	1569336895	Effect of Articulatory Δ and ΔΔ Parameters on Multilayer Neural Network based Speech Recognition
		Manoj Banik; Mohammed Rokibul Alam Kotwal; Foyzul Hassan; Gazi Md. Moshfiqul Islam; Sharif Mohammad Musfiqur Rahman; Mohammad Mahedi Hasan; Ghulam Muhammad; Mohammad Huda
15.00 pm - 15.20 pm	1569335443	Dynamic Wordlength Calibration to Reduce Power Dissipation in Wireless OFDM Systems
		Jaeseong Kim; Shingo Yoshizawa; Yoshikazu Miyanaga
15.20 pm - 15.40 pm	1569335395	Adaptive Blind System Identification for Speech Dereverberation Using a Priori Estimates
		Rajan Rashobh; Andy W. H. Khong; Patrick A Naylor
RM3-S4 Sentral Accord & Network Room (Hilton Kuala Lumpur) MEMS System		
Session Chair: Prof. Prakash R. Apte		
16.00 pm - 16.20 pm	1569319359	A Study on Characteristic and Reliability of Fabricated Microfluidic Three Electrodes Sensor Based on Randle-Sevcik Equation
		Imi Hamiza Hamzah; Asrulnizam Abd Manaf; Othman Sidek
16.20 pm - 16.40 pm	1569327651	Design, Simulation, Modeling and Characterization of Micromachined Microcantilever using CoventorWare Software
		Abdelaziz Yousif Ahmed; John Ojur Dennis; Mohamad Naufal Mohamad Saad
16.40 pm - 17.00 pm	1569341465	A 8-Resistor SU-8 Accelerometer with Reduced Cross Axis Sensitivity
		V. Ramgopal Rao; Prasenjit Ray; Prakash R Apte
17.00 pm - 17.20 pm	1569336851	Design and Modeling of MEMS Resonator for Magnetic Field Sensing using hybrid actuation technique
		Farooq Ahmad; John Dennis; Nor Hisham Hamid; Mohd Haris Md Khir; Abdelaziz Yousif Ahmed

The IEEE APCCAS 2010, the 11th biennial Asia Pacific Conference on Circuits and Systems, will be held in Malaysia in the splendid five-star Hilton Kuala Lumpur and Le Meridien Kuala Lumpur hotels with a superb location only a stone's throw away from the shopping and entertainment hub surrounded by an exciting potpourri from *Truly Asia*, consists of Malay, Chinese, Indian, Eurasian and European. The APCCAS is a major international forum established by the IEEE Circuits and Systems Society for researchers to exchange their latest findings in circuits and systems.

Tutorials: The tutorials will be held on Monday 6th December 2010. Please submit proposals for tutorial sessions to the tutorial chair.

Special sessions: Proposals are solicited for special sessions. Please submit proposals for special sessions to the special sessions chair.

Paper submissions: Complete 4-page manuscript (in standard IEEE double-column format), including title, authors' names, affiliations and e-mail addresses, and a short abstract are requested. Papers must be submitted electronically in PDF format. Only electronic submission will be accepted. For detailed information, please consult the conference website: **http://www.apccas2010.org**

The IEEE APCCAS 2010 is a meeting place for scholars, scientists, educators, students, engineers, entrepreneurs and managers. It covers a wide range of topics including, but not limited to the following:

Conference Focus Topics

- Analog Signal Processing
- Biomedical Engineering
- Blind Signal Processing
- Cellular Neural Networks and Array Computing
- Circuits and Systems for Communications
- Circuits and Systems Education and Outreach
- Computer-Aided Network Design
- Digital Signal Processing
- Life-Science Systems and Applications
- Multimedia Systems and Applications
- Nanoelectronics and Gigascale Systems
- Neural Systems and Applications
- Nonlinear Circuits and Systems
- Power Systems and Power Electronic Circuits
- Sensory Systems
- Visual Signal Processing and Communications
- Test Technology
- System-on-Chip (SOC)
- Packaging
- MEMS Technology

Important Dates

Deadline for submission of Tutorial Proposals:	20 June 2010
Deadline for submission of Special Sessions Proposals:	10 June 2010
Notification of acceptance of Tutorial Proposals:	30 June 2010
Notification of acceptance of Special Sessions Proposal:	15 June 2010
Deadline for submission of Full 4-page Papers in Regular Sessions:	30 June 2010
Deadline for submission of Full 4-page Papers in Special Sessions:	10 July 2010
Notification of Paper Acceptance:	15 August 2010
Deadline for submission of FINAL Papers:	10 September 2010
Deadline for Author and Early-Bird Registration:	10 September 2010
Conference Dates:	6-9 Dec 2010

Keynote Speakers

Randall Geiger
Iowa State university

Shoji Kawahito
Shizuoka University

Ljiljana Trajkovic
Simon Fraser University

Ramesh Harjani
University of Minnesota

Enrico Macii
Politecnico di Torino

David Skellern
National Information and Communications Technology Australia LTD

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國科會補助計畫衍生研發成果推廣資料表

日期:2011/08/30

國科會補助計畫	計畫名稱: 應用於多輸入多輸出偵測系統之K-Best球型解碼演算法實現
	計畫主持人: 林光浩
	計畫編號: 99-2221-E-167-033- 學門領域: 積體電路及系統設計

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：林光浩	計畫編號：99-2221-E-167-033-
計畫名稱：應用於多輸入多輸出偵測系統之 K-Best 球型解碼演算法實現	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	4	4	100%		參加研討會有2011Symposium on Engineering, Medicine and Biology Applications，The 22nd VLSI Design/CAD Symposium，The 6th Intelligent Living Technology Conference
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	1	1	100%		The IEEE APCCAS 2010, the 11th biennial Asia Pacific Conference on Circuits and Systems
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	4	4	100%	人次	
		博士生	0	0	100%		

		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

下世代的無線通訊網路，主要是由多輸入多輸出系統與正交分頻多工系統所架構而成。正交分頻多工非常適合寬頻傳輸系統，而多輸入多輸出技術主要在傳送與接收端使用多根天線，因此可以增加資料傳輸速度且利用空間處理能增加對空間使用效率。為了達到最佳的最大相似度偵測效能，運算複雜度將會隨著調變群集大小而增加，也隨著傳送天線數目大小而呈指數型增加。球型編碼演算法主要是為了改善 ML 太過複雜的演算法而產生的，但其仍有變動的複雜度與資料輸出量的不利因素存在。而一般的 K-Best 球型編碼演算法主要能提供固定的資料輸出量，但其仍有效能衰減的問題存在。一般來說，當 K 值越大，就越趨近最大相似度的偵測效能，但是也會有高複雜度與大量的功率消耗問題存在著。