國立勤益技術學院九十三學年度研究所招生初試試題卷

所別：資訊與電能科技研究所　組別：資訊科技組　身分別：一般生及在職生

科目：電子學　准考證號碼：□□□□□□□□（考生自填）

考生注意事項：

一、考試時間 100 分鐘。

二、請先核對考試科目與報考所組別是否相符。

三、本試題共六題，每題分數列於題後，共 100 分，請依序作答。

四、答案須寫在答案卷上，本試題空白處或背面，僅做計算或草稿使用。

五、考生不可攜帶計算機、翻譯機或通信器設備等作答。

六、請在試題首頁准考證號碼之方格內，填上考生本人之准考證號碼。作答完畢後，請將「答案卷」及「試題」一併繳回。

1. The 6.8V zener diode in the circuit of Fig. 1 is specified to have V_Z=6.8V at I_Z=5mA, r_z=20Ω, and I_{ZK}=0.2mA. The supply voltage V^+ is normally 10V but can vary by ±1V.

   (a) Find V_o with no load and with V^+ at its nominal value. (5%)

   (b) Find the change in V_o resulting from the ±1V change in V^+. (5%)

   (c) Find the change in V_o resulting from connecting a load resistance R_L=2kΩ. (5%)

   (d) Find the value of V_o when R_L=0.5kΩ. (5%)

   (e) What is the minimum value of R_L for which the diode still operates in the break-down region? (5%)

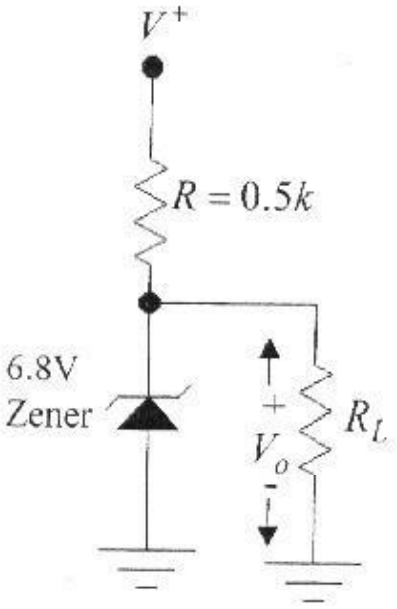

Fig. 1(a)

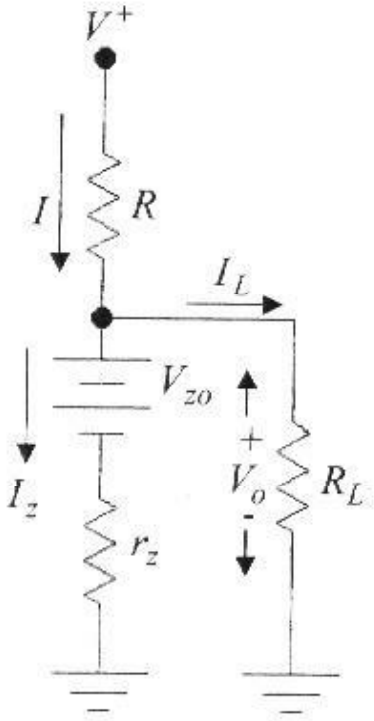

Fig. 1(b)

2. Fig. 2 shows two circuits for generating a constant current $I_o = 10\mu A$. Determine the values of the required resistors (R_1, R_2, R_3) assuming that V_{BE} is 0.7V at a current of 1 mA (I_{ref}) and neglecting the effect of finite β. (15%)

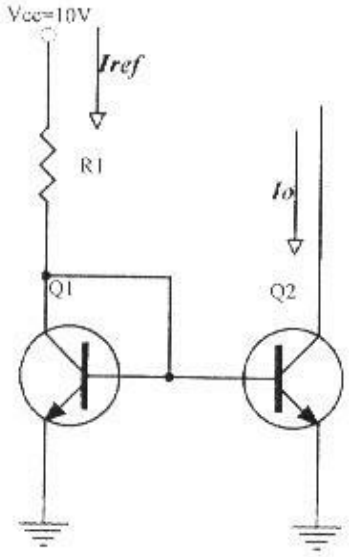

Fig. 2(a)

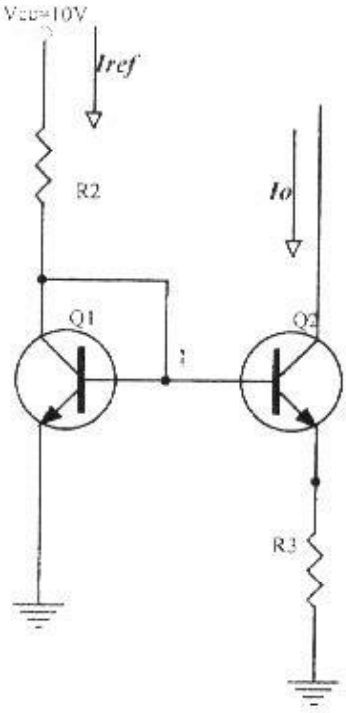

Fig. 2(b)

3. Determine the voltage gain V_O/V_S for the noninverting Op-Amp stage in Fig.3 by first evaluating A_D, A_{OL}, T, and K. (20%)

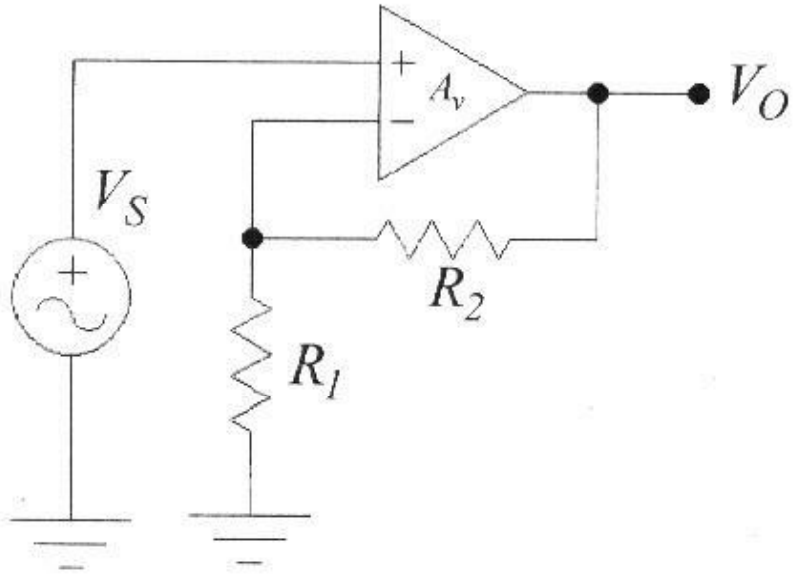

Fig. 3

4. Fig. 4 is a sample of a 4 bits D/A converter using a binary-weighted resistive ladder network. Please sketch the equivalent network by using R-2R ladders? (15%)

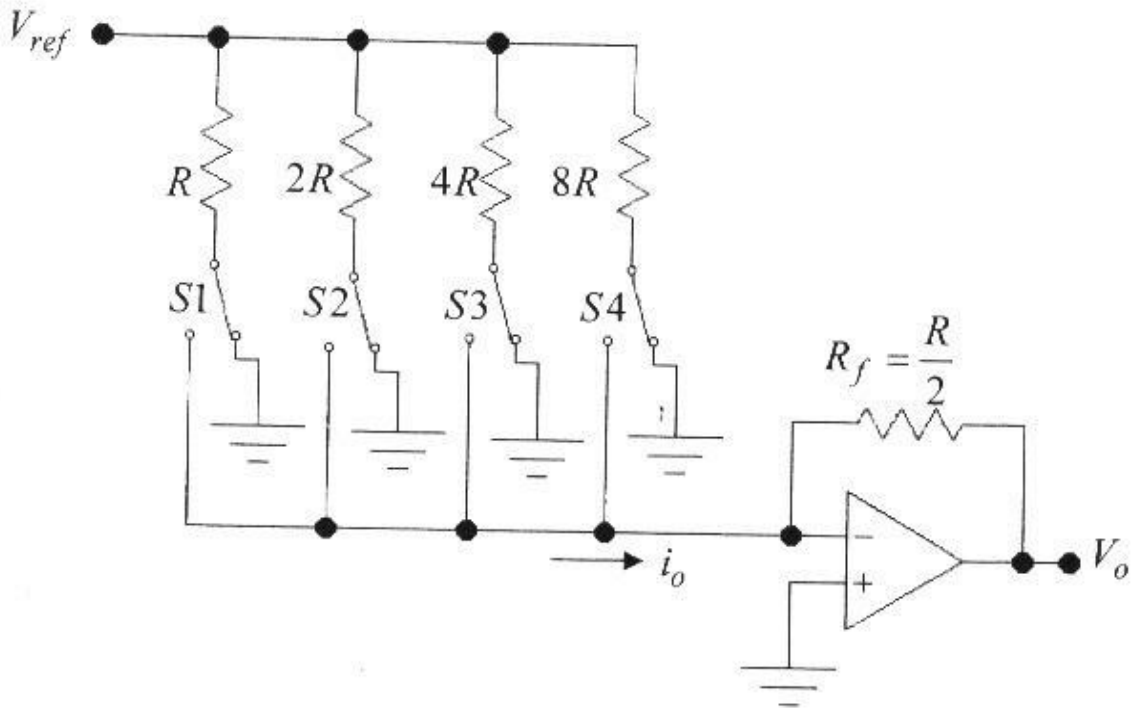

Fig. 4

5. Sketch the waveform of the definitions of propagation delays (t_p) and switching times ($t_r, t_f, t_{PHL}, t_{PLH}, t_{THL}, t_{TLH}$) of the logic inverter. (15%)

6. Draw the circuit diagram of a simple instrument amplifier by using one Op-Amp. Write an expression for the output voltage (V_O) of this circuit in terms of the input voltages (V_1, V_2) and circuit resistances. (10%)