Hindawi Publishing Corporation
Mathematical Problems in Engineering
Volume 2013, Article ID 598130, 13 pages
http://dx.doi.org/10.1155/2013/598130

Research Article

Mathematical Modeling and Fault Tolerance Control for a Three-Phase Soft-Switching Mode Rectifier

Kuei-Hsiang Chao and Chin-Tsang Hsieh

Department of Electrical Engineering, National Chin-Yi University of Technology, No. 57, Section 2, Zhongshan Road, Taiping District, Taichung 41170, Taiwan

Correspondence should be addressed to Kuei-Hsiang Chao; chaokh@ncut.edu.tw

Received 10 October 2012; Revised 13 December 2012; Accepted 14 December 2012

Academic Editor: Zheng-Guang Wu

This study primarily focuses on the design of an intelligent three-phase soft-switching mode rectifier (SSMR). Firstly, the small-signal dynamic model of a single-phase SSMR is derived together with the design of its controller. Then, the developed single-phase SSMR is connected to form an intelligent three-phase SSMR. When any of the phase modules in the proposed intelligent three-phase SSMR experiences a fault, it can continue to supply power automatically under reduced load capacity while still maintaining good power quality characteristics. Finally, some simulation results were used to demonstrate the effectiveness of the proposed intelligent three-phase SSMR design.

1. Introduction

Traditional rectifiers contain a large amount of harmonic currents, which reduce the power factor of input AC side and greatly deteriorate the power quality. To enhance power quality, a switching-mode rectifier (SMR) with power factor regulation [1] is used to make the rectifier-induced current form a sine wave with the power factor near to 1. A traditional hard-switch mode SMR comes with reduced power conversion efficiency due to a larger switching loss and possesses greater switching stress and electromagnetic interference (EMI). It uses the auxiliary resonant branches connected to the original power circuit on the hard-switching mode SMR and the modified switching control signals of the pulse-width modulation (PWM) to complete the soft-switching mode rectifier (SSMR) operation [2]. In general, large electrical equipments are fed with a three-phase power. A considerable variety of three-phase circuit configurations have been derived from single-phase switching rectifier circuits. Among them, the circuit architecture of a boost converter [3–5] is the simplest in form, easiest to control, and superior in performance; these are the primary reasons for its wide use. To date, a variety of circuit configurations and control technologies for the single-stage three-phase boost AC/DC converter have been proposed. Some of these configurations use a single active switch [6, 7], while others use six active switches [8, 9]. Single active switch-based three-phase boost AC/DC converters have a very simple architecture but contain a large amount of low older harmonics. Six active switch-based three-phase boost AC/DC converters can obtain a better power factor and harmonic control characteristics but involve a more complex control strategy.

Some three-phase SMRs constructed using three or two separate single-phase SMR modules were presented in [10–13]. Though the three connected single-phase modules in a three-phase Δ-connected SMR [12] can directly apply the power factor control and soft-switching technology of a single-phase module, when one of the three-phase modules fails, Δ-connected can change to V-connected. It can continue to provide power under a reduced load condition, which translates into improved system reliability, but it is done at the expense of power quality [12]. In [13], the authors proposed a modified T-connected three-phase SMR, which is constructed using two single-phase SMRs and one center-tapped autotransformer. The three-phase line drawn currents are made balanced by applying unbalanced two-phase voltages to power the two-single SMRs. However, as any module is randomly disabled, this three-phase SMR

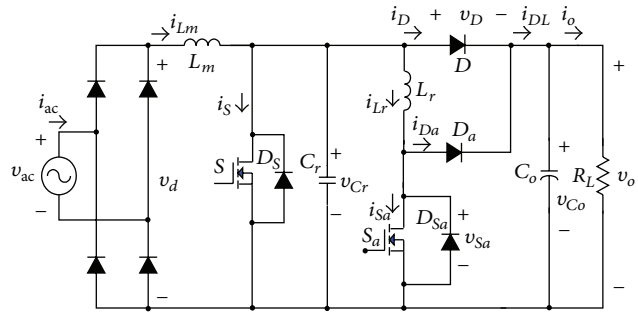

Figure 1: Circuit configuration of the proposed ZVT SSMR.

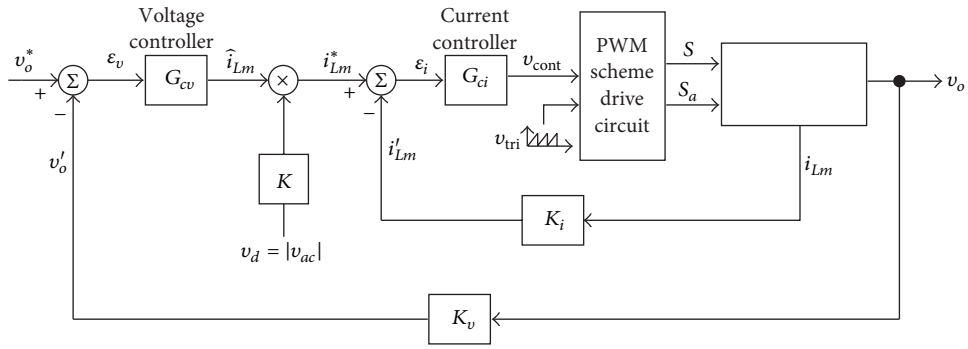

Figure 2: Block diagram of the control structure of the proposed ZVT SSMR.

cannot online detect the fault occurrence and continuously perform the three-phase SMR operation through automatic switch connection arrangement. To overcome these problems, this study proposes that single-phase SSMR modules should be connected together to form an intelligent three-phase SSMR that not only has a simple connection structure but also possesses automatic online fault detection functions. In the case of a module experiencing a fault, the intelligent three-phase SSMR can continue to maintain the three-phase balance of high power quality electricity supply without having to shut down for fault module maintenance, thus greatly enhancing the quality and reliability of the power supplied by the system.

2. Single-Phase SSMR

Figure 1 shows the power circuit of the single-phase boost SSMR adopted in this study. The proposed zero-voltage transition (ZVT) SSMR system design adopts the current switch control method that uses ramp-comparison pulse-width modulation under the continuous current conduction mode (CCM).

2.1. Scheme of Control Loop. The control block diagram of the proposed SSMR, as shown in Figure 2, contains both inner and outer control loops. The inner loop is the current control loop, and the outer loop is the voltage control loop. The role of the current control loop is to raise the power factor, and the role of the voltage control loop is to provide stability control for the output DC voltage.

According to the on- and off-states of circuit switches and diodes in Figure 1, a switching period can be divided into seven operating modes. Their main waveform variables are as shown in Figure 3.

2.2. Design of a Current Control Loop Controller. The state average method can be used to derive the current loop gain transfer function [10]. If the current controller $G_{ci}(s)$ chooses to use a proportional-integrated (PI) controller, then the general rule of the crossover frequency of current control loop gain should be less than the switching frequency 1/2 (i.e., $f_c < 0.5 f_s$) and should be applied for the design of the current controller [10], which obtains

$$G_{ci}(s) = \frac{K_{Pi}s + K_{Ii}}{s} = \frac{16.5s + 10000}{s}. \quad (1)$$

2.3. Deriving the Converter Model. The ZVT SSMR circuit configuration in Figure 1 was divided into a slow-variable subsystem and a fast-variable subsystem [14]. The slow subsystem consisted of main storage (filter) components for input and output, while the fast subsystem consisted of resonant components with a state variable filter (slow system variables) as $i_{Lm}(t)$ and $v_{Co}(t)$ and resonant state variables (fast system variables) as $i_{Lr}(t)$ and $v_{Cr}(t)$. From the fast subsystem perspective, the slow state variables in the entire switching period T_s could be considered as constants. In contrast, from the slow subsystem perspective, only the average effect of fast resonant state variables could be seen. Therefore, when deriving the mathematical model for the converter, the moving average function of the fast variables

Table 1: $v_{Cr}(t)$, $i_D(t)$, and $i_{Da}(t)$ solutions for SSMR in the seven operation modes.

Time period	Variable		
	$v_{Cr}(t)$	$i_D(t)$	$i_{Da}(t)$
$T_1 : [t_0 \sim t_1]$	$v_{Co}(t)$	$i_{Lm}(t) - [v_{Co}(t)/Lr](t - t_0)$	0
$T_2 : [t_1 \sim t_2]$	$v_{Co}(t) \cos \omega_o(t - t_1)$	0	0
$T_3 : [t_2 \sim t_3]$	0	0	0
$T_4 : [t_3 \sim t_4]$	0	0	$i_{Lm}(t) + v_{Co}(t)/Z_o + [v_{Co}(t)/Lr](t - t_3)$
$T_5 : [t_4 \sim t_5]$	0	0	0
$T_6 : [t_5 \sim t_6]$	$[i_{Lm}(t)/C_r](t - t_5)$	0	0
$T_7 : [t_6 \sim t_0]$	$v_{Co}(t)$	$i_{Lm}(t)$	0

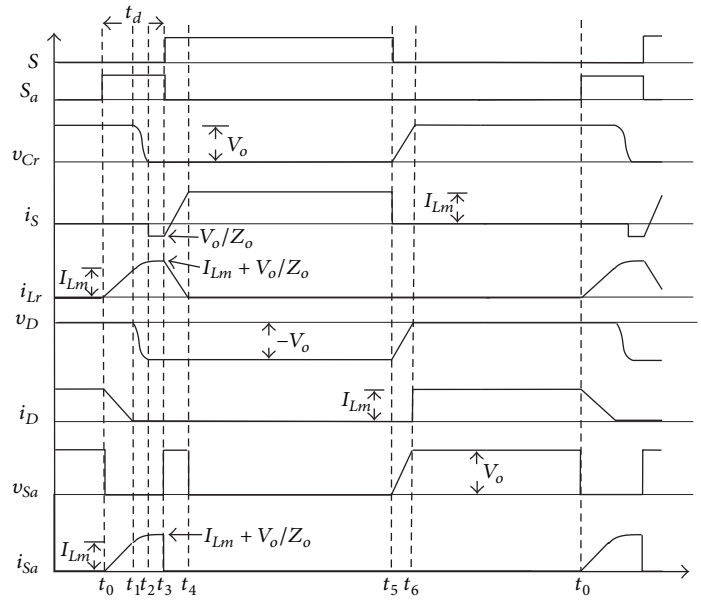

Figure 3: Voltage and current waveforms of the main components of ZVT SSMR.

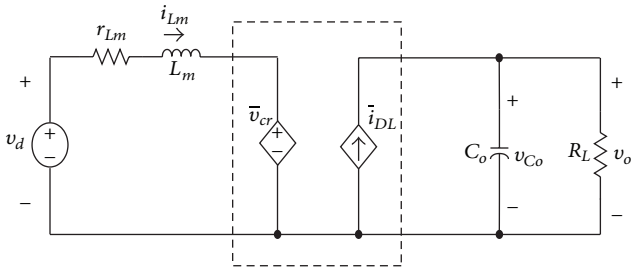

Figure 4: Average equivalent circuit from a slow speed perspective.

should be calculated first and then substituted into the slow variables to obtain the averaging model for the slow variables. Finally, the average power method was used to derive the small-signal model of the converter [15]. From the circuit configuration in Figure 1, the slow filter perspective could be used to depict the average equivalent circuit of the slow system that was shown in Figure 4. The dashed-line portion indicates the average effect of fast variables on the slow variables system. Additionally, r_{Lm} is the serial equivalent resistance of the boost inductor L_m.

Then, the voltage v_{Cr} of the resonant capacitor C_r and the moving average function of the sum $i_{DL} = i_D + i_{Da}$ of the currents i_D and i_{Da} flowing through both the diode D and the auxiliary diode D_a were separately obtained. The seven operation modes [10] in Figure 3 were used to obtain v_{Cr}, i_D, and i_{Da} under various mode solutions, listed in Table 1. The results listed in Table 1 could be used to separately obtain the moving average function of v_{Cr} and i_{DL}.

(a) Obtain moving average function $\bar{v}_{Cr}$ of v_{Cr} as

$$\bar{v}_{Cr}(t) = \langle v_{Cr}(t) \rangle_{T_s} = \frac{1}{T_s} \sum_{i=0}^{6} \int_{t_i}^{t_{i+1}} v_{Cr}(\tau)\, d\tau. \quad (2)$$

(b) Obtain moving average function $\bar{i}_{DL}$ of $i_{DL}(t)$ as

$$\bar{i}_{DL}(t) = \langle i_{DL}(t) \rangle_{T_s} = \frac{1}{T_s} \sum_{i=0}^{6} \int_{t_i}^{t_{i+1}} [i_D(t) + i_{Da}(t)]\, d\tau. \quad (3)$$

Since the system in Figure 1 shows a very small loss to be negligible, the averaged equivalent circuit of the slow system

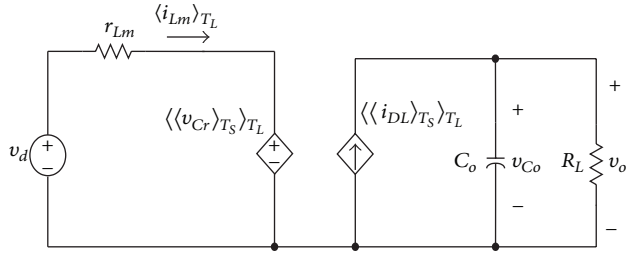

Figure 5: Slow speed perspective average model equivalent circuit during the period T_L of input voltage v_d.

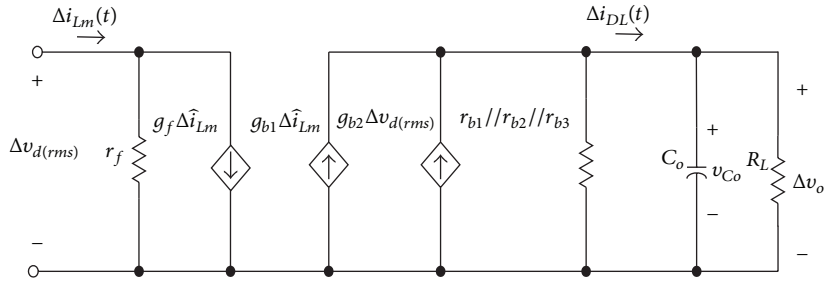

Figure 6: Small-signal equivalent circuit model of the converter.

shown in Figure 4 can be plotted like Figure 5. Its average value of $\bar{i}_{DL}(t)$ during the input voltage period T_L is

$$\begin{aligned}\left\langle \bar{i}_{DL}(t)\right\rangle_{T_L} &\triangleq \left\langle \left\langle i_{DL}(t)\right\rangle_{T_s}\right\rangle_{T_L}\\ &= \frac{K_1^2\pi^2 L_r \hat{i}_{Lm}^2 v_{d(rms)}^2}{8T_s v_o} + \frac{K_1 L_r \hat{i}_{Lm} v_{d(rms)}}{T_s Z_o}\\ &\quad + \frac{K_1\pi \hat{i}_{Lm} v_{d(rms)}^2}{2\sqrt{2}v_o} - \frac{C_r v_o}{2T_s},\end{aligned} \tag{4}$$

where $K_1 = 2\sqrt{2}K/\pi$, and K is the proportional constant of the rectifier.

At the DC operating point of $\langle i_{Lm}\rangle_{T_L} = I_{Lm}$, $v_{d(rms)} = V_{d(rms)}$, $\hat{i}_{Lm} = \hat{I}_{Lm}$, $\langle \bar{i}_{DL}(t)\rangle_{T_L} = I_{DL}$, and $v_o = V_o$, after experiencing a small-signal disturbance and ignoring high-order terms of AC, the system can obtain the following.

(a) The AC component of the input current $\langle i_{Lm}\rangle_{T_L}$ is

$$\begin{aligned}\Delta i_{Lm}(t) &= K_1 V_{d(rms)}\Delta\hat{i}_{Lm}(t) + K_1\hat{I}_{Lm}\Delta v_{d(rms)}(t)\\ &\triangleq g_f\Delta\hat{i}_{Lm}(t) + \frac{1}{r_f}\Delta v_{d(rms)}(t),\end{aligned} \tag{5}$$

where $g_f \triangleq K_1 v_{d(rms)}$, and $r_f \triangleq 1/(K_1\hat{I}_{Lm})$.

(b) AC component of output current $\langle \bar{i}_{DL}(t)\rangle_{T_L}$ is

$$\begin{aligned}\Delta i_{DL}(t) &= g_{b1}\Delta\hat{i}_{Lm}(t) + g_{b2}\Delta v_{d(rms)}(t)\\ &\quad - \left[\frac{1}{r_{b1}} + \frac{1}{r_{b2}} + \frac{1}{r_{b3}}\right]\Delta v_o(t),\end{aligned} \tag{6}$$

where

$$\begin{aligned}g_{b1} &\triangleq \frac{K_1\pi V_{d(rms)}^2}{2\sqrt{2}V_o} + \frac{K_1^2\pi^2 L_r \hat{i}_{Lm} V_{d(rms)}^2}{4T_s V_o}\\ &\quad + \frac{K_1 L_r V_{d(rms)}}{T_s Z_o},\\ g_{b2} &\triangleq \frac{K_1\pi \hat{I}_{Lm} V_{d(rms)}}{\sqrt{2}v_o} + \frac{K_1^2\pi^2 L_r \hat{I}_{Lm}^2 V_{d(rms)}}{4T_s V_o}\\ &\quad + \frac{K_1 L_r \hat{I}_{Lm}}{T_s Z_o},\\ r_{b1} &\triangleq \frac{2\sqrt{2}V_o^2}{K_1\pi\hat{I}_{Lm}V_{d(rms)}^2} = \frac{2\sqrt{2}V_o^2}{\pi I_{Lm} V_{d(rms)}},\\ r_{b2} &\triangleq \frac{8T_s V_o^2}{K_1^2\pi^2 L_r \hat{I}_{Lm}^2 V_{d(rms)}^2} = \frac{8T_s V_o^2}{\pi^2 L_r I_{Lm}^2},\\ r_{b3} &\triangleq \frac{2T_s}{C_r}.\end{aligned} \tag{7}$$

Equations (5) and (6) can be used to draw the small-signal equivalent circuit model of the converter, as shown in Figure 6. The transfer function of $\Delta\hat{i}_{Lm}$ to Δv_o when $\Delta v_{d(rms)} = 0$ can be derived from Figure 6 as follows:

$$\begin{aligned}&\left.\frac{\Delta v_o(s)}{\Delta\hat{i}_{Lm}(s)}\right|_{(\Delta v_{d(rms)}=0)}\\ &= \frac{g_{b1}\times\left(R_L/\left(1+sR_L C_o\right)\right)}{1+\left[\left(1/\left(r_{b1}//r_{b2}//r_{b3}\right)\right)\times\left(R_L/\left(1+sR_L C_o\right)\right)\right]}\\ &= \frac{g_{b1}R_{_L}}{sR_L C_o + \left(R_L/\left(r_{b1}//r_{b2}//r_{b3}\right)\right)+1}.\end{aligned} \tag{8}$$

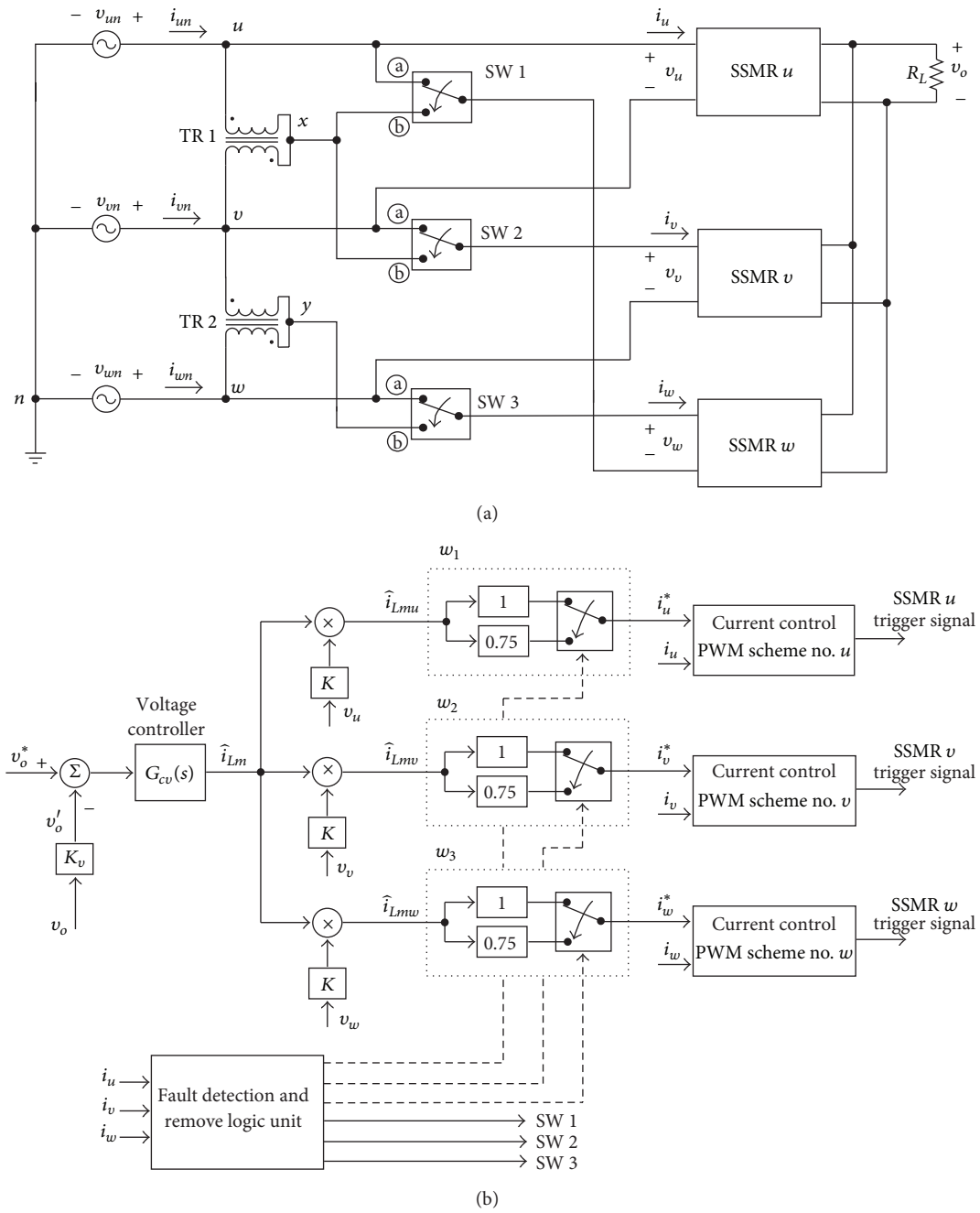

FIGURE 7: The proposed intelligent three-phase SSMR: (a) circuit configuration; (b) control structure.

3. Proposed Intelligent Three-Phase SSMR

The three-phase rectifier circuit system possesses advantages such as higher capacity, higher output voltage ripple frequency, and smaller ripple amplitude. Therefore, to increase the system capacity and the quality of the power supply, the single-phase SSMR in this study is connected to form a three-phase SSMR for the power supply. When any of the phase modules experiences a fault, the three-phase SSMR system can continue to maintain the three-phase balanced power supply under a reduced load capacity while still maintaining excellent power quality characteristics.

3.1. Proposed Circuit Configuration of a Single-Phase SSMR Module Connected to Form a Three-Phase SSMR. The proposed circuit configuration and control structure of the intelligent three-phase SSMR has two more center-tapped autotransformers and three more toggle switches than a traditional three-phase Δ-connected SSMR system, as shown in Figures 7(a) and 7(b) [13, 16]. The control structure of the intelligent three-phase SSMR in Figure 7(b) has added current distributing factors $w_1 \sim w_3$, fault diagnosis, and troubleshooting logic components. The fault diagnosis and troubleshooting logic unit controlled the switching of the proposed intelligent three-phase SSMR toggle switches

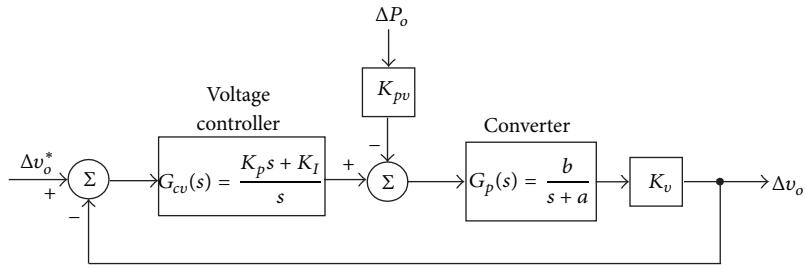

Figure 8: Voltage control loop block diagram of the proposed three-phase SSMR.

SW1~SW3 and the selection of current distribution factors $w_1 \sim w_3$. SW1~SW3 in each module switche to the ⓐ point shown in Figure 7(a) under normal operation, with the selection of current distribution factors $w_1 \sim w_3$ as 1. When each module of the proposed intelligent three-phase SSMR is operating under normal conditions, its circuit configuration is complete the same as the three-phase Δ-connected SSMR. Therefore, the total capacity and the phasor diagram of voltage and current of the intelligent three-phase SSMR are similar to those of a traditional three-phase Δ-connected SSMR.

3.2. Design of a Voltage Control Loop Controller. Under good current tracking characteristics, the proposed voltage control loop of a three-phase SSMR can be reasonably expressed as in the block diagram of Figure 8, where K_{pv} is the conversion coefficient of a load power disturbance on the voltage, K_v is the expressed voltage sensing conversion factor, which is set as $K_v = 0.02(V/V)$, and $G_p(s)$ is the transfer function of the converter. Based on the ease of implementation consideration, the voltage controller $G_{cv}(s)$ uses a PI controller.

The proposed small-signal equivalent circuit model for the three-phase SSMR converter is plotted in Figure 9 based on the single-phase SSMR determined in Section 2.3. The transfer function of $\Delta\widehat{i}_{Lm}$ to Δv_o during $\Delta v_{d(rms)} = 0$ that can be obtained from Figure 9 is

$$\left.\frac{\Delta v_o(s)}{\Delta \widehat{i}_{Lm}(s)}\right|_{(\Delta v_{d(rms)}=0)} = \frac{3g_{b1} \times (R_L/(1+sR_LC_o))}{1+[(3/(r_{b1}//r_{b2}//r_{b3})) \times (R_L/(1+sR_LC_o))]} = \frac{3g_{b1}R_L}{sR_LC_o + (3R_L/(r_{b1}//r_{b2}//r_{b3})) + 1}. \quad (9)$$

When the module load in each phase reaches $P_o = 300.4$ W, the voltage controller will first use a simple proportional controller (P-controller) $G_{cv}(s) = K_p = 5$ and set v_o^* to 8 V (the actual command value is 8 V/0.02 = 400 V). In cases where the input inductor current $i_{Lm}(t)$ is able to completely track the command current, the current amplitude command signal $\widehat{I}_{Lm}$ is measured to be 6.4 A, with an actual output voltage of 360 V at the specific moment. The rest of the parameters required for seeking the transfer function of the converter are listed in Table 2. By substituting the parameters listed in Table 2 into (9), the converter transfer function can be obtained as

$$G_p(s) = \frac{b}{s+a} = \frac{851.38}{s+20.16}. \quad (10)$$

Table 2: Parameters required for finding the transfer function of the converter.

Input voltage $V_{d(rms)}$	220 V
Maximum output power P_o	600 W
Boost inductor L_m	450 μH
Output filter capacitor C_o	2000 μF
Load resistor R_L	150 Ω
Resonant inductor L_r	20 μH
Resonant capacitor C_r	870 PF
Switching period T_s	10 μs
Resonant impedance Z_o	151.62 Ω
Ratio constant K_r	5 V/220 V

If the system is to achieve high performance load regulation characteristics, the step load dynamic response is generally required to possess characteristics such as zero steady-state error, zero overshoot, smallest possible maximum voltage dip, and quickest possible restore time. The output voltage specification requirements on the step response are

(i) steady-state error = 0;

(ii) overshoot = 0;

(iii) output voltage dip caused by a unit-step load change $\Delta P_o = 600$ W is set to $\Delta v_{o,\max} = 8$ V;

(iv) voltage dip restore time: $t_r = 0.8$ sec.

The voltage controller parameters that can be obtained using voltage controller quantitative design steps [15] are $K_p = 1.3$ and $K_I = 9.46$.

3.3. Power Supply Situation during Any Phase Fault in the Proposed Intelligent Three-Phase SSMR. The circuit configuration and the phasor diagram of the associated voltage and current of the proposed intelligent three-phase SSMR during u phase module failure are shown in Figure 10. Assume that when the u phase SSMR module is experiencing a fault, the position of SW3 will be switched to ⓑ, and at that specific moment, the output power values of SSMR v and SSMR w are

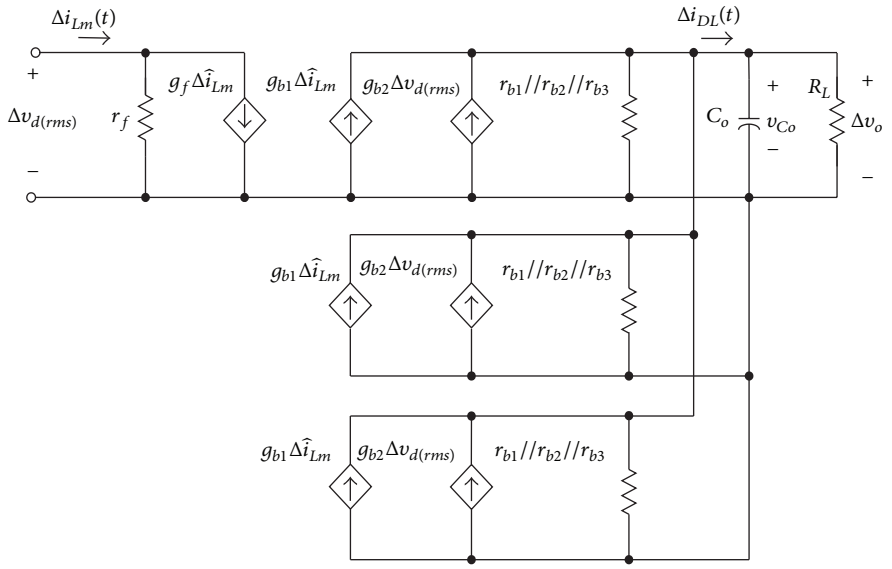

Figure 9: Small-signal equivalent circuit model of the proposed three-phase SSMR converter.

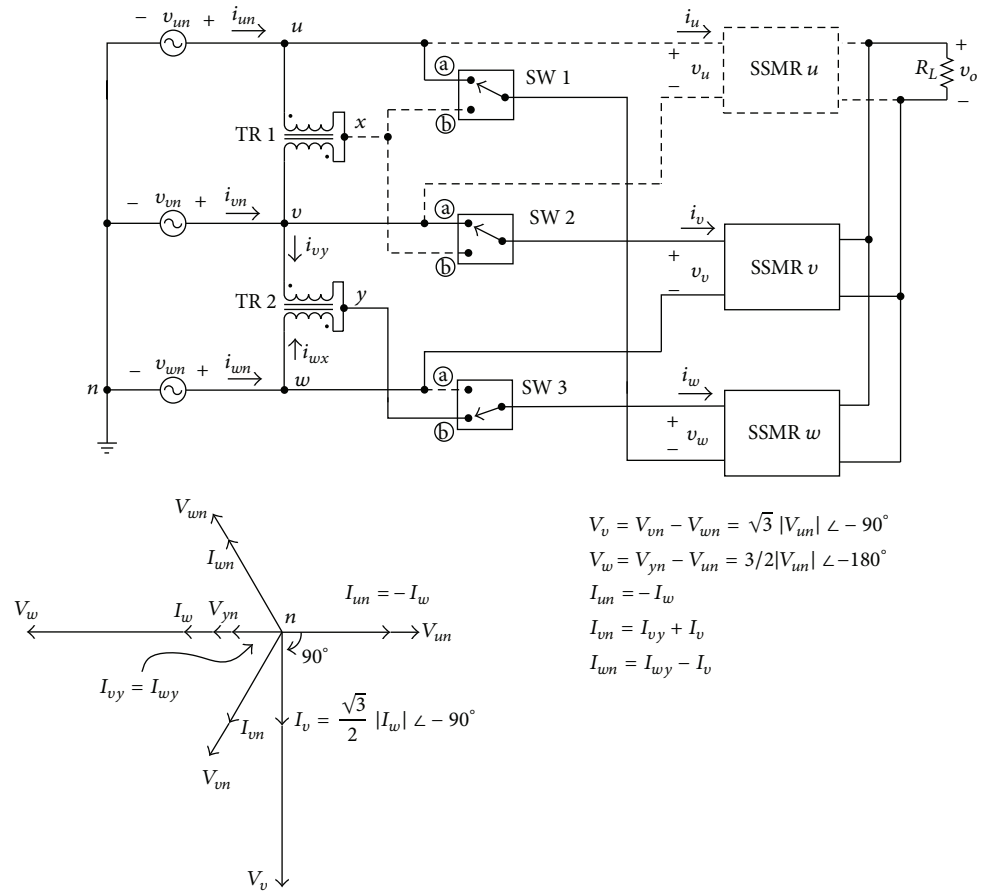

Figure 10: The circuit configuration and the phasor diagram of related voltages and currents of the proposed intelligent three-phase SSMR during u phase fault.

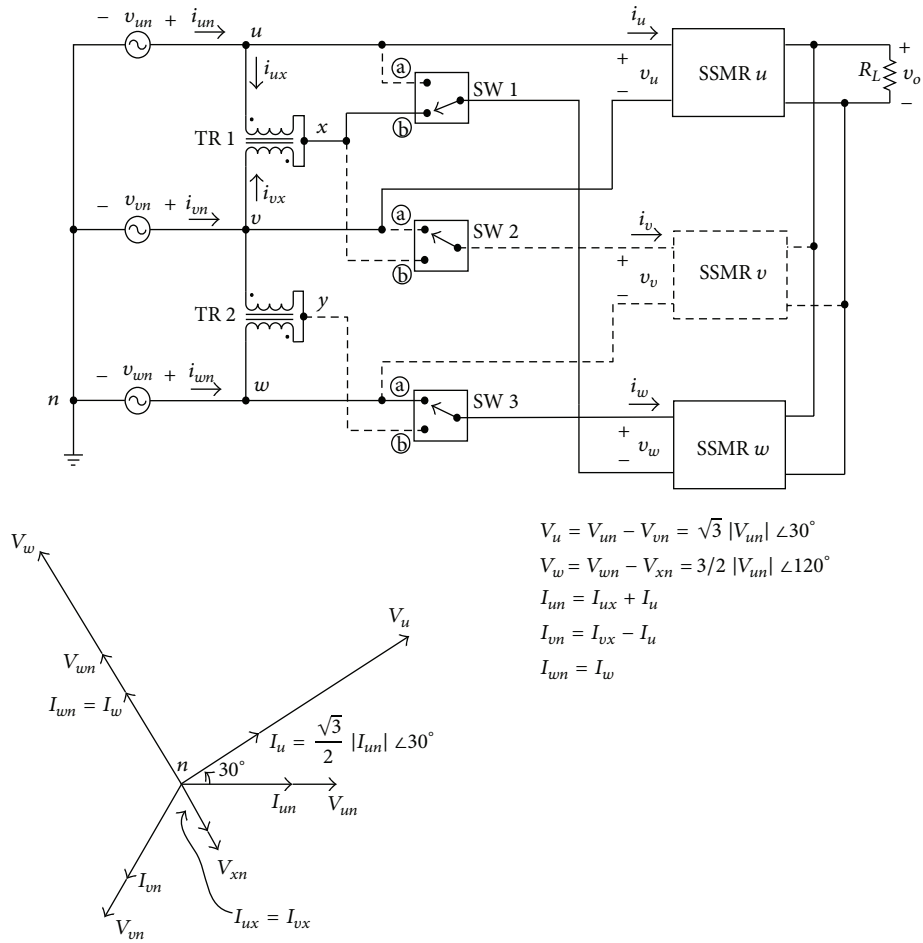

Figure 11: The circuit configuration and the phasor diagram of related voltages and currents of the proposed intelligent three-phase SSMR during v phase fault.

P_v and P_w. Their circuit configuration and the phasor diagram of related voltages and currents are plotted in Figure 10, and the obtained P_v and P_w are

$$P_v = |V_v|\,|I_v| = \left(\sqrt{3}\,|V_{un}|\right)\left(K\sqrt{3}\,|V_{un}|\,\hat{i}_{Lm}w_2\right),$$
$$P_w = |V_w|\,|I_w| = \left(\frac{3}{2}\,|V_{un}|\right)\left(K\frac{3}{2}\,|V_{un}|\,\hat{i}_{Lm}w_3\right), \tag{11}$$

where K is the proportionality constant of the rectifier, and w_2 and w_3 are current distribution factors of SSMR v and SSMR w, respectively. In (11), the purported $P_v = P_w$ condition must be met by satisfying

$$w_2 : w_3 = 0.75 : 1. \tag{12}$$

At the moment when $|V_v| = V$, $|I_v| = (\sqrt{3}/2)I$, $|V_W| = (\sqrt{3}/2)V$, and $|I_W| = I$, the total capacity of the proposed modified T-connected SSMR during a fault in SSMR u is

$$VA_T = P_T = |V_v|\,|I_v| + |V_W|\,|I_W| = \sqrt{3}VI = \frac{1}{\sqrt{3}}P_\Delta. \tag{13}$$

When a fault occurs in the v phase SSMR module, the output power values of SSMR u and SSMR w are P_u and P_w.

The circuit configuration and the phasor diagram of the related voltages and currents are plotted in Figure 11, and the obtained P_u and P_w are

$$P_u = |V_u|\,|I_u| = \left(\sqrt{3}\,|V_{un}|\right)\left(K\sqrt{3}\,|V_{un}|\,\hat{i}_{Lm}w_1\right),$$
$$P_w = |V_w|\,|I_w| = \left(\frac{3}{2}\,|V_{un}|\right)\left(K\frac{3}{2}\,|V_{un}|\,\hat{i}_{Lm}w_3\right), \tag{14}$$

where K is the proportionality constant of the rectifier, and w_1 and w_3 are current distribution factors of SSMR u and SSMR w, respectively. In (14), the purported $P_u = P_w$ condition must be met by satisfying

$$w_1 : w_3 = 0.75 : 1. \tag{15}$$

At the moment when $|V_u| = V$, $|I_u| = (\sqrt{3}/2)I$, $|V_W| = (\sqrt{3}/2)V$, and $|I_W| = I$, the total capacity of the proposed modified T-connected SSMR during a fault in SSMR v is

$$VA_T = P_T = |V_u|\,|I_u| + |V_W|\,|I_W| = \sqrt{3}VI = \frac{1}{\sqrt{3}}P_\Delta. \tag{16}$$

When a fault occurs in a w phase SSMR module, the output power values of SSMR u and SSMR v are P_u and

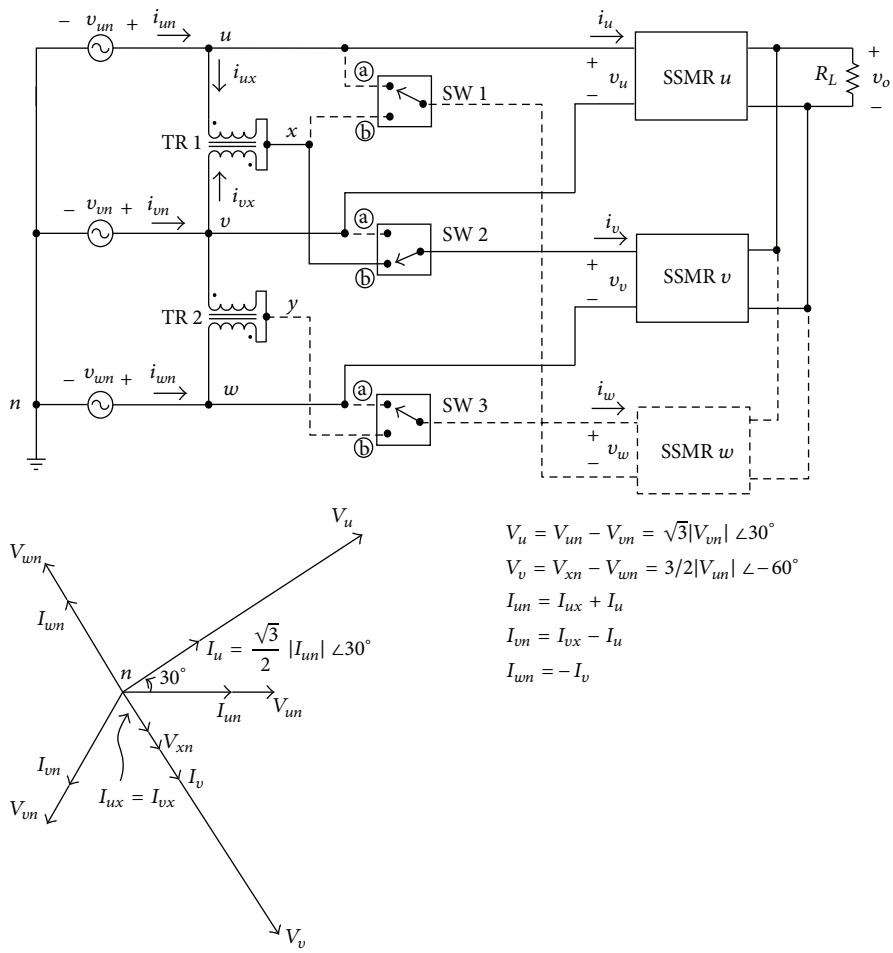

FIGURE 12: The circuit configuration and the phasor diagram of related voltages and currents of the proposed intelligent three-phase SSMR during w phase fault.

P_v. The circuit configuration and the phasor diagram of the correlated voltages and currents are plotted in Figure 12, and the obtained P_u and P_v are

$$P_u = |V_u||I_u| = \left(\sqrt{3}|V_{un}|\right)\left(K\sqrt{3}|V_{un}|\widehat{i}_{Lm}w_1\right),$$
$$P_v = |V_v||I_v| = \left(\frac{3}{2}|V_{un}|\right)\left(K\frac{3}{2}|V_{un}|\widehat{i}_{Lm}w_2\right), \quad (17)$$

where K is the proportionality constant of the rectifier, and w_1 and w_2 are current distribution factors of SSMR u and SSMR v, respectively. In (17), the purported $P_u = P_v$ condition must be met by satisfying

$$w_1 : w_2 = 0.75 : 1. \quad (18)$$

At the moment when $|V_u| = V$, $|I_u| = (\sqrt{3}/2)I$, $|V_v| = (\sqrt{3}/2)V$, and $|I_v| = I$, the total capacity of the proposed modified T-connected SSMR during a fault in SSMR w is

$$VA_T = P_T = |V_u||I_u| + |V_v||I_v| = \sqrt{3}VI = \frac{1}{\sqrt{3}}P_\Delta. \quad (19)$$

Based on the previous analysis, when a fault occurs in any phase module of the proposed intelligent three-phase SSMR, the total capacity is reduced to $1/\sqrt{3}$ that of normal operation. When a fault occurs to any phase module and during normal three-phase module operation, the switch state of toggle switches SW1~SW3 and the current distribution factors used in each module are as shown in Tables 3 and 4. During normal operation, current flowing through the module can be detected; therefore, the logic level of that module during normal operation is set to high. In contrast, when a module experiences a fault, the logic level is set to low. In Table 3, when the switch is placed at the ⓐ point, the logic level is set to high. When it is at the ⓑ point, it is set to low. In Table 4, when the current distribution factor is 1, the logic

TABLE 3: Positions of toggle switches SW1~SW3 under various operating conditions.

Operating condition	Switch		
	SW1	SW2	SW3
Normal operation	ⓐ	ⓐ	ⓐ
SSMR u fault	ⓐ	ⓐ	ⓑ
SSMR v fault	ⓑ	ⓐ	ⓐ
SSMR w fault	ⓐ	ⓑ	ⓐ

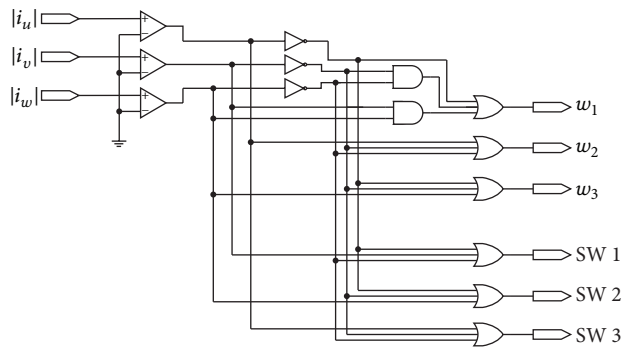

FIGURE 13: Logic control circuit of the proposed intelligent three-phase SSMR.

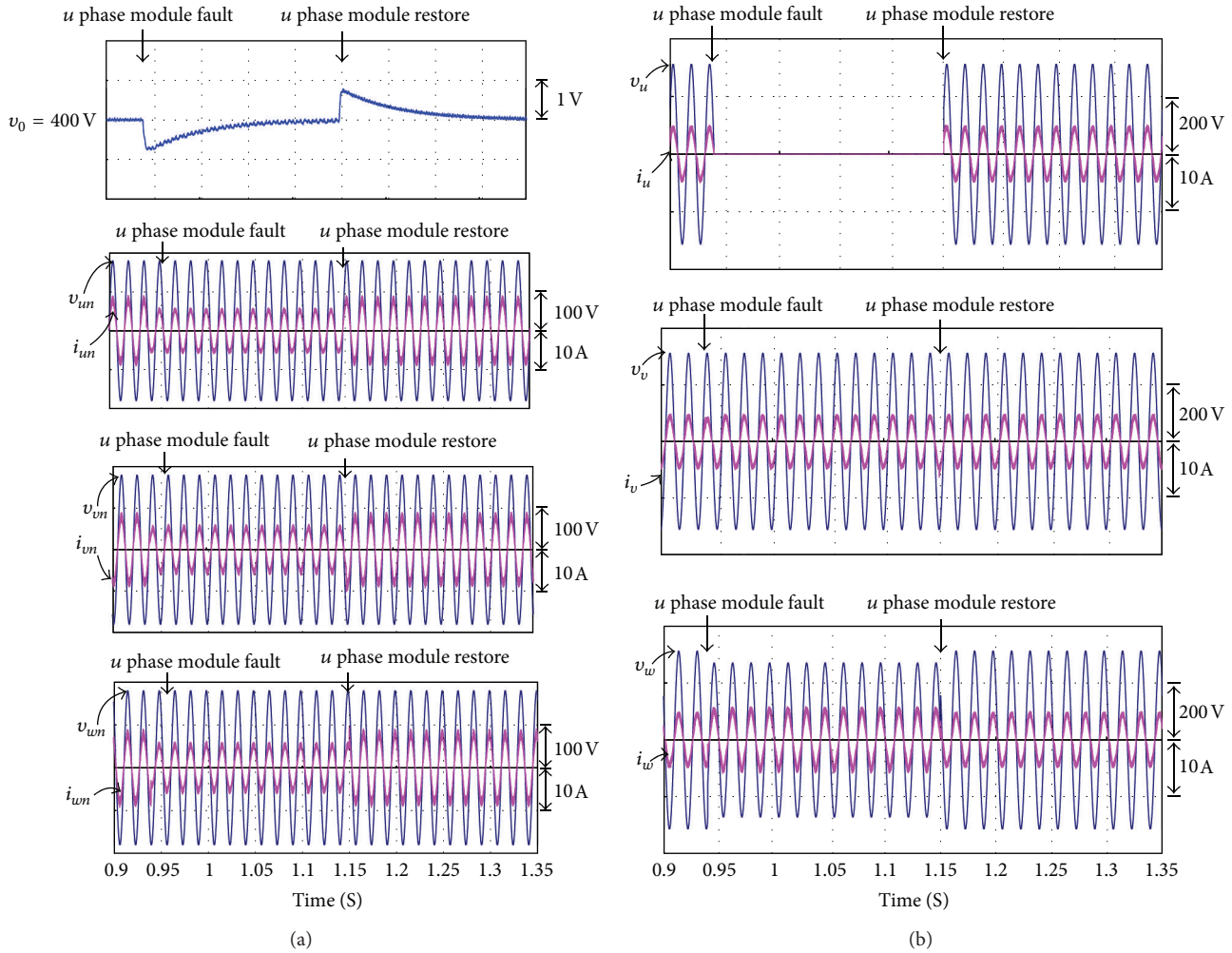

FIGURE 14: Simulated results of a continuous power supply when the load drops from 1800 W to $1800/\sqrt{3}$ W during a failure of a SSMR u module in the proposed intelligent three-phase SSMR: (a) simulated waveforms of output DC voltages and input voltages and currents for each phase; (b) simulated waveforms of input voltages and currents of various modules.

level is set to high; when the current distribution factor is 0.75, the logic level is set to low. The logic levels demonstrated by the previous results are summarized in a logic control circuit truth-value table in Table 5. The truth-value table listed in Table 5 has been simplified using Karnaugh map, and its logic control circuit can be realized using the logic circuit in Figure 13. The logic circuit in Figure 13 can be used to control the position of the toggle switches SW1~SW3 and the selection of a current distribution factor in Figures 10 to 12. When a fault occurs in any phase module of the proposed three-phase modified T-connected SSMR system, the detected faulty module can again perform a no-fault module current distribution factor selection and can automatically toggle the position of switches SW1~SW3 to

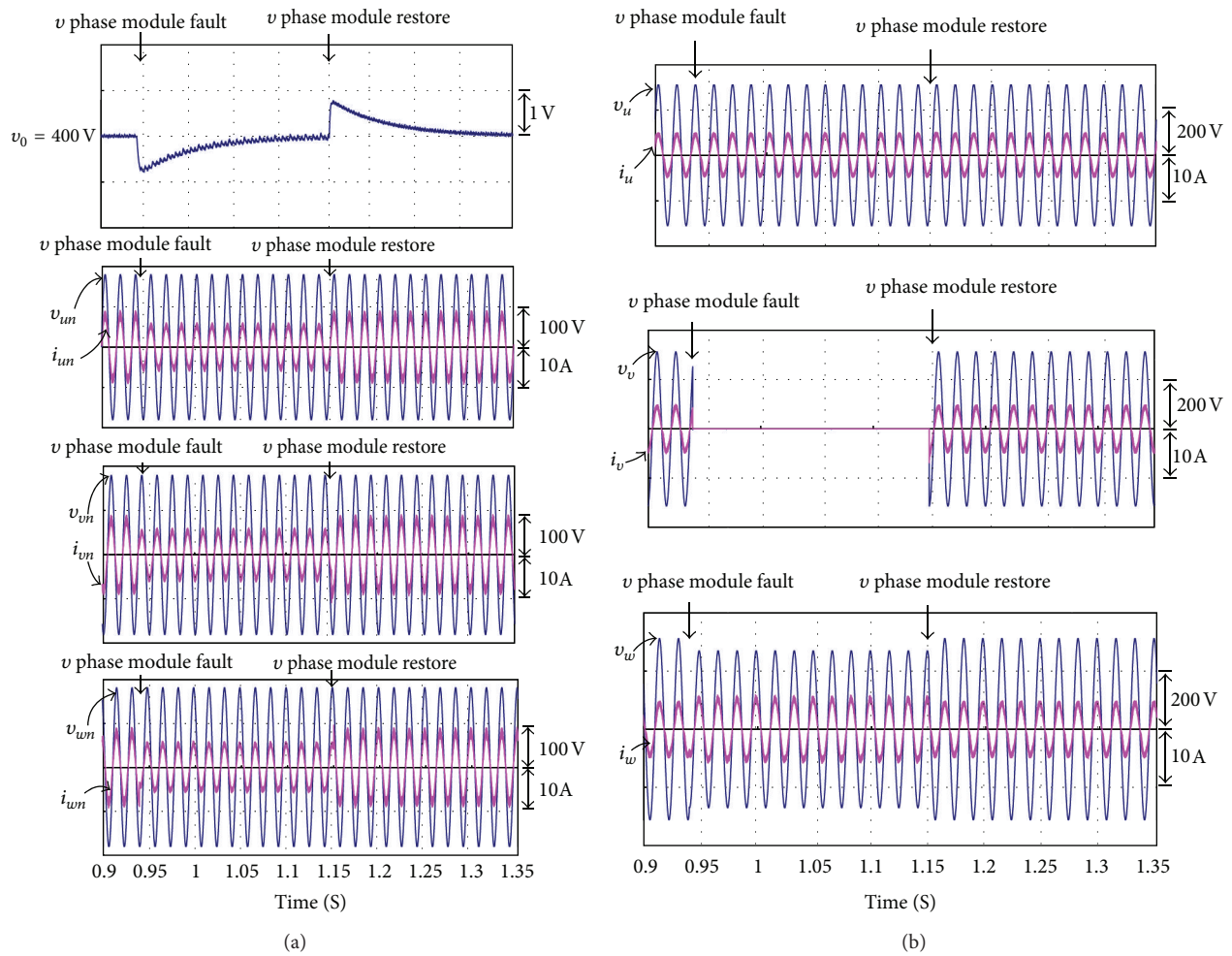

Figure 15: Simulated results of a continuous power supply when the load drops from 1800 W to $1800/\sqrt{3}$ W during a failure of a SSMR υ module in the proposed intelligent three-phase SSMR: (a) simulated waveforms of output DC voltages and input voltages and currents for each phase; (b) simulated waveforms of input voltages and currents of various modules.

Table 4: Current distribution factors used under various operating conditions.

Operating condition	Current distribution factor		
	w_1	w_2	w_3
Normal operation	1	1	1
SSMR u fault	×	0.75	1
SSMR υ fault	0.75	×	1
SSMR w fault	0.75	1	×

Note: × indicates not taking into consideration.

change the circuit configuration. The three-phase balanced power supply is continuously maintained under a reduced load capacity, allowing it to still regulate the input voltage and current into almost the same phase. This achieves an excellent supply quality of almost 1.0 in the power factor.

4. Simulation Results of the Proposed Intelligent Three-Phase SMR

Since each single module of the proposed intelligent three-phase SSMR system is rated at 600 W, the total power is 1800 W. Therefore, when a fault occurs in any module in this system, if the load capacity is greater than $1800/\sqrt{3}$ W, then the system reduces the load to continue providing power. This ensures that no-fault modules would not be burnt down by a power overload. Figures 14, 15, and 16 are the PSIM software generated waveforms representing relevant restored voltages and currents after the troubleshooting of faults from a sudden failure of any of the SSMR u, SSMR υ, and SSMR w modules under a reduced power load when the proposed SSMR supply load is 1800 W. As is evident from the intelligent three-phase SSMR shown in the figures, when each module is operating normally, the three-phase input line voltage and current are nearly in phase to produce a three-phase balance power supply. When one module fails, the input line voltage and current of the three-phase can maintain in phase and supply the three-phase balance power, while the amplitude of the input voltage and current and phasor diagram of each no-fault module is also consistent with positions that are in phase. Therefore, it has a good power factor and low harmonic characteristics. The output DC voltage during the dynamic response to a module fault and the post fault troubleshooting

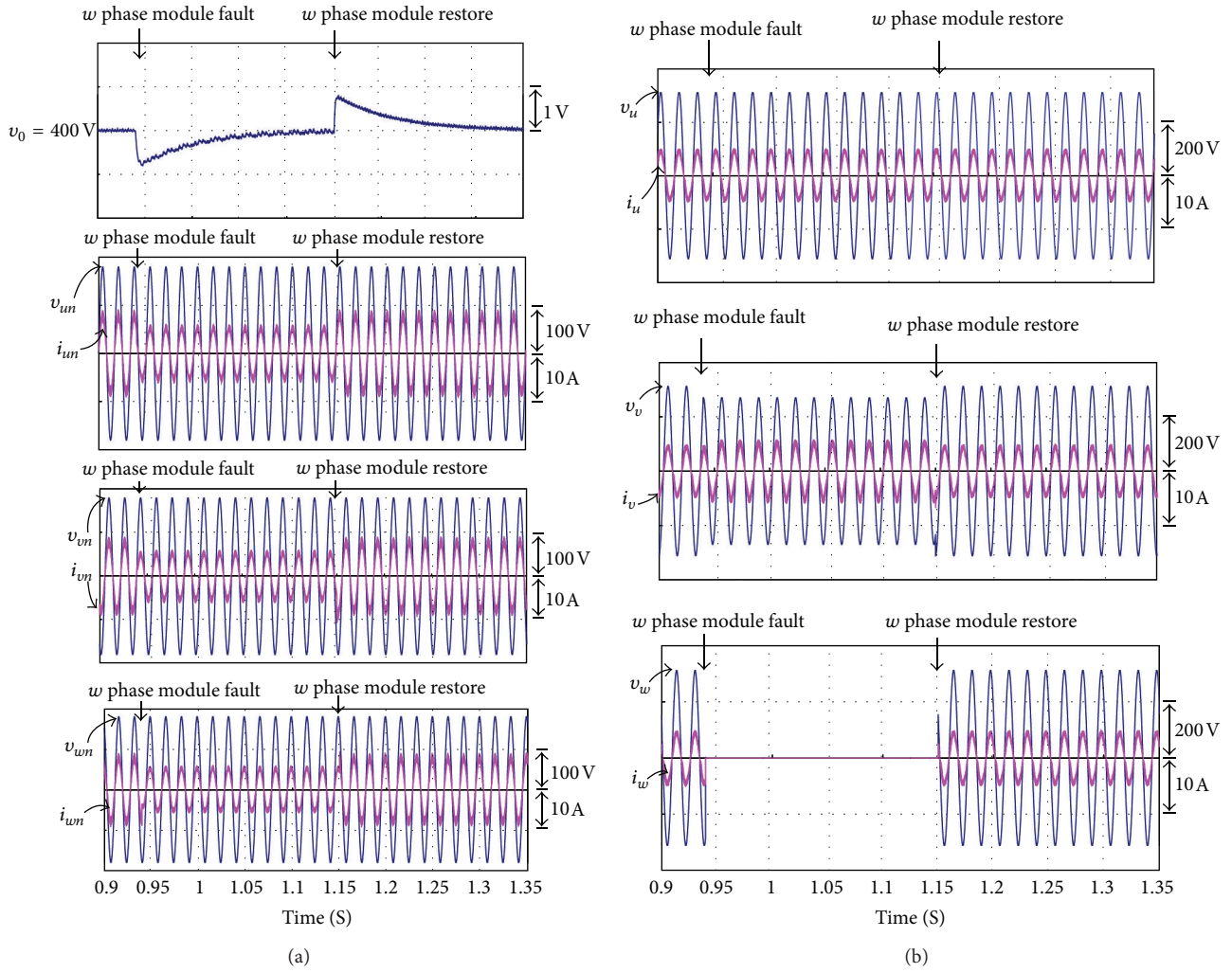

FIGURE 16: Simulated results of a continuous power supply when the load drops from 1800 W to $1800/\sqrt{3}$ W during a failure of SSMR w module in the proposed intelligent three-phase SSMR: (a) simulated waveforms of output DC voltages and input voltages and currents for each phase; (b) simulated waveforms of input voltages and currents of various modules.

TABLE 5: Truth-value table of a logic control circuit of the proposed intelligent three-phase SSMR.

$\|i_u\|$	$\|i_v\|$	$\|i_w\|$	w_1	w_2	w_3	SW1	SW2	SW3
L	L	L	×	×	×	×	×	×
L	L	H	H	H	H	H	H	H
L	H	L	H	H	H	H	H	H
L	H	H	×	L	H	H	H	L
H	L	L	H	H	H	H	H	H
H	L	H	L	×	H	L	H	H
H	H	L	L	H	×	H	L	H
H	H	H	H	H	H	H	H	H

power restoration can also use the designed voltage controller to retain a high regulation performance.

The comparisons of circuit structure, switching characteristics, power quality, fault tolerance, and reliability of the power supply between the proposed three-phase SSMR and some of the existing ones are made in Table 6. It shows that the proposed three-phase SSMR possesses the advantages of flexibility, reliability, superior power quality, and on-line fault detection tolerance.

5. Conclusions

For the application of a three-phase power feeding in large-capacity power electronic equipment, this study adopted single-phase single module SSMR to assemble an intelligent three-phase SSMR system power supply. When any module in this three-phase SSMR module experiences a fault, the proposed intelligent three-phase SSMR system can use intelligent online fault diagnosis and a fault troubleshooting strategy to immediately reduce the load capacity online to continue maintaining the three-phase balanced power supply, keeping the three-phase SSMR system from shutting down for rerouting. This greatly enhances the reliability of the power supply, while the three-phase input voltage and current

Table 6: Characteristics comparison between different three-phase switching mode rectifiers (SMRs).

Items	Topologies		
	TSP PFC SMR in [13]	PFC SSMR in [12]	Proposed SSMR
Circuit structure	Medium	Simple	Medium
Switching characteristics	Hard-switching	Soft-switching	Soft-switching
Power quality	Superior	Inferior	Superior
Fault tolerance	Inferior	Inferior	Superior
Reliability of the power supply	Inferior	Inferior	Superior

are still almost in phase; so, the power supply side can still possess the characteristics of good power factor and low harmonics.

References

[1] J. Sebastian, M. Jaureguizar, and J. Uceda, "Overview of power factor correction in single-phase off-line power supply systems," in *Proceedings of the 20th International Conference on Industrial Electronics, Control and Instrumentation (IECON '94)*, pp. 1688–1693, September 1994.

[2] G. Hua, C. S. Leu, Y. Jiang, and F. C. Y. Lee, "Novel zero-voltage-transition PWM converters," *IEEE Transactions on Power Electronics*, vol. 9, no. 2, pp. 213–219, 1994.

[3] D. Weng and S. Yuvarajan, "Resonant-boost-input three-phase power factor corrector using IGBT switches with ZCS switching condition," in *Proceedings of the IEEE Industry Applications Conference*, pp. 2526–2529, October 1999.

[4] C. Qiao and K. M. Smedley, "A general three-phase PFC controller for rectifiers with a parallel-connected dual boost topology," *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 925–934, 2002.

[5] Y. Nishida, Y. Ohgoe, M. Nakaoka, and A. Maeda, "Simple three-phase boost-mode PFC rectifier," in *Proceedings of the IEEE IAC*, pp. 1056–1061, October 1996.

[6] M. S. Dawande and G. K. Dubey, "Programmable input power factor correction method for switch-mode rectifiers," *IEEE Transactions on Power Electronics*, vol. 11, no. 4, pp. 585–591, 1996.

[7] I. H. Oh and D. S. Lee, "Single-switched PWM resonant converter for a three-phase boost rectifier," in *Proceedings of the 30th Annual IEEE Power Electronics Specialists Conference (PESC '99)*, pp. 676–680, July 1999.

[8] R. Zhang, S. Hiti, F. C. Lee, and D. Boroyevic, "Three-phase ZVT boost rectifier with improved analog controller," in *Proceedings of the 27th Annual IEEE Power Electronics Specialists Conference (PESC '96)*, pp. 469–474, January 1996.

[9] P. Ide, N. Froehleke, and H. Grotstollen, "Comparison of selected 3-phase switched mode rectifiers," in *Proceedings of the 19th International Telecommunications Energy Conference (INTELEC '97)*, pp. 630–636, October 1997.

[10] M. Hengchun, C. Y. Lee, D. Boroyevich, and S. Hiti, "Review of high-performance three-phase power-factor correction circuits," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 4, pp. 437–446, 1997.

[11] B. N. Singh, P. Jain, and G. Joos, "Three-phase AC/DC regulated power supplies: a comparative evaluation of different topologies," in *Proceedings of the 15th Annual IEEE Applied Power Electronics Conference and Exposition (APEC '00)*, pp. 513–518, February 2000.

[12] K. H. Chao, "Modeling and control of soft-switching mode rectifiers with power factor correction," *Journal of the Chinese Institute of Engineers*, vol. 33, no. 3, pp. 437–449, 2010.

[13] J. Hahn, P. N. Enjeti, and I. J. Pitel, "A new three-phase power-factor correction (PFC) scheme using two single-phase PFC modules," *IEEE Transactions on Industry Applications*, vol. 38, no. 1, pp. 123–130, 2002.

[14] S. H. Li, *Development of switching-mode rectifiers: modeling, control, and multi-module operations [Ph.D. thesis]*, Department of Electrical Engineering, National Tsing-Hua University, 2004.

[15] C. M. Liaw, "Design of a two-degree-of-freedom controller for motor drives," *IEEE Transactions on Automatic Control*, vol. 37, no. 8, pp. 1215–1220, 1992.

[16] J. L. Lin and C. H. Chang, "Small-signal modeling and control of ZVT-PWM boost converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 2–10, 2003.