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Research Article

A High-Efficiency Monolithic DC-DC PFM Boost Converter with Parallel Power MOS Technique

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This paper presents a high-efficiency monolithic dc-dc PFM boost converter designed with a standard TSMC 3.3/5V 0.35 μm CMOS technology. The proposed boost converter combines the parallel power MOS technique with pulse-frequency modulation (PFM) technique to achieve high efficiency over a wide load current range, extending battery life and reducing the cost for the portable systems. The proposed parallel power MOS controller and load current detector exactly determine the size of power MOS to increase power conversion efficiency in different loads. Postlayout simulation results of the designed circuit show that the power conversion is 74.9–90.7% efficiency over a load range from 1 mA to 420 mA with 1.5 V supply. Moreover, the proposed boost converter has a smaller area and lower cost than those of the existing boost converter circuits.

1. Introduction

The great demands for portable electronic equipment, such as cellular phones, personal digital assistants (PDAs), digital cameras, and hand-held communication instruments are growing rapidly in the huge consumer markets [1–10]. The utilization of single-cell battery in the portable devices is increasing to reduce effectively the volume and weight of the products. Increasing the power efficiency of the converter is important to extend the lifetime of battery. Several popular techniques [1–7] have been extensively implemented.

The pulse width modulation (PWM) technique is frequently adopted in the literature [3, 5–7]. The switching converter in PWM mode had high power efficiency and low ripple voltage operated in the heavy load. Unfortunately, when the switching converter is operated under medium-to-light loads, its power efficiency is seriously degraded. The fixed-frequency PWM suffers in this way because the switching loss dominates the total power loss with medium-to-light loads. The pulse-frequency modulation (PFM) technique in discontinuous-conduction mode (DCM) [1, 8] has been used to increase the power efficiency under the medium-to-light load conditions. The load current determined the switching frequency of switching converters with PFM technique. Thus, the lower switching frequency in PFM mode effectively reduced the switching loss under the medium-to-light loads. Some commercial dc-dc converters [2, 4] combined PWM and PFM techniques to get high power efficiency from heavy load to light load operations. Moreover, a segmented output stage for optimized efficiency, proposed by Trescases et al., has been used in PWM technique [8]. Although the proposed circuit [8] had a 7.5% better efficiency under medium-to-light loads, it had high cost, and large areas were needed.

This paper proposes a novel load current detector and parallel power MOS technique that accurately adjust the number of parallel power MOS transistors used based on the load conditions, to achieve high power efficiency. The proposed scheme yields a smaller area and lower cost than all other existing schemes [2–9], because it depends on external compensated components. The proposed boost converter is designed with a standard TSMC 3.3/5V 0.35-μm 2P4M CMOS technology. The postlayout simulation results show

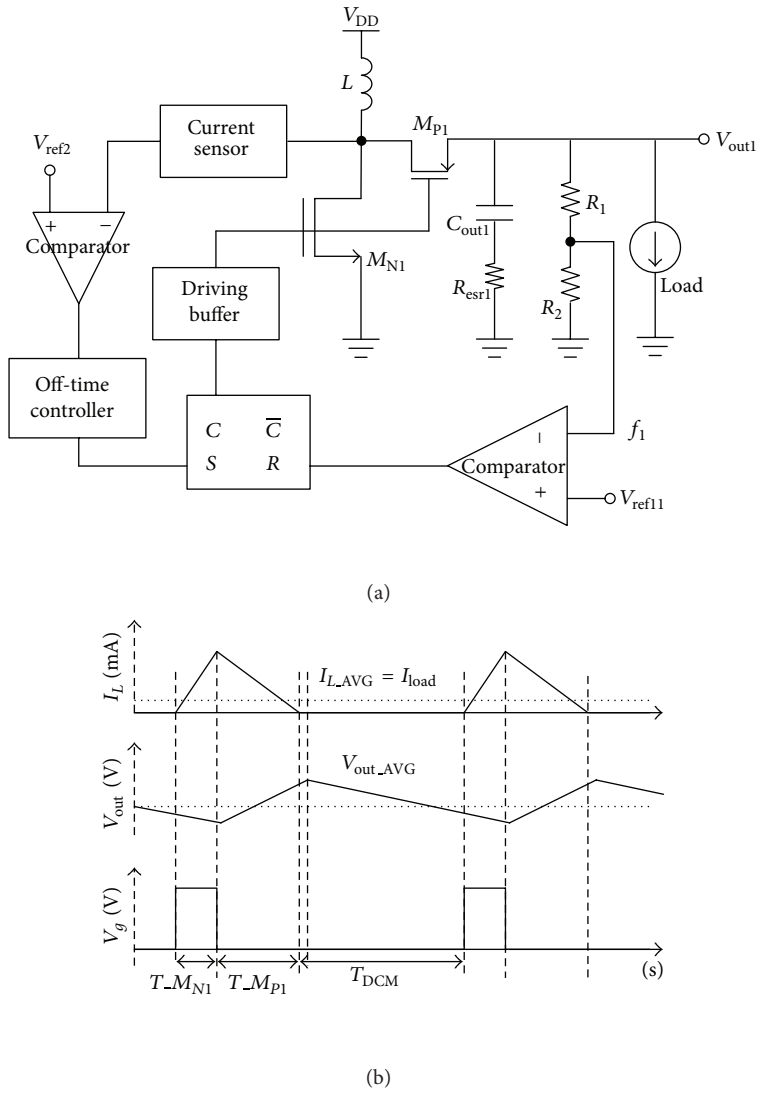

Figure 1: (a) Schematic PFM dc-dc boost converter; (b) key waveforms of discontinuous-conduction mode (DCM).

that the power efficiency of the proposed boost converter from 1 mA to 420 mA output current exceeds 74.9% at a 1.5 V supply.

The remainder of this paper is organized as follows. Section 2 describes the existing pfm dc-dc boost converters. Section 3 presents the proposed high-efficiency monolithic dc-dc boost converter with parallel power MOS. Section 4 presents simulation results that confirm the effectiveness of the proposed circuit. The final section draws conclusions.

2. The Existing PFM DC-DC Boost Converter

Figure 1(a) schematically depicts an existing PFM dc-dc boost converter. It consists of the power stage and PFM technique circuits which contain a current sensor, a driving buffer, an off-time controller, an SR latch, and comparators. The switching converter in PFM mode has high power efficiency when operated under the medium-light load conditions because the PFM technique is always utilized in the discontinuous-conduction mode (DCM) to reduce the switching loss. Figure 1(b) displays the key waveforms of DCM where the on-time (T_M_{N1}) of the power transistor M_{N1} is fixed and the T_{DCM} varies with the load current. T_{DCM} is inversely proportional to the load. During T_{DCM}, both switches M_{N1} and M_{P1} remain off and the load current is supplied by the output capacitor C_{out1}.

3. The Proposed DC-DC PFM Boost Converter

In this paper, a novel dc-dc PFM boost converter is designed to maintain high power-conversion efficiency of the converter for portable applications over large load ranges. Figure 2 presents the block diagram of the proposed dc-dc PFM boost converter that comprises a parallel power PMOS/NMOS, a load current detector, a parallel power MOS controller, an energy time generator, and a sense current detector. When the load circuit operates in the standby or

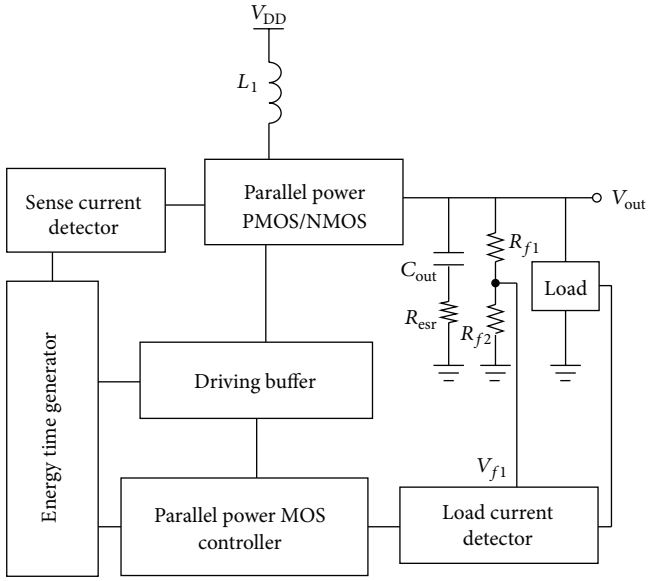

Figure 2: Block diagram of proposed PFM dc-dc boost converter.

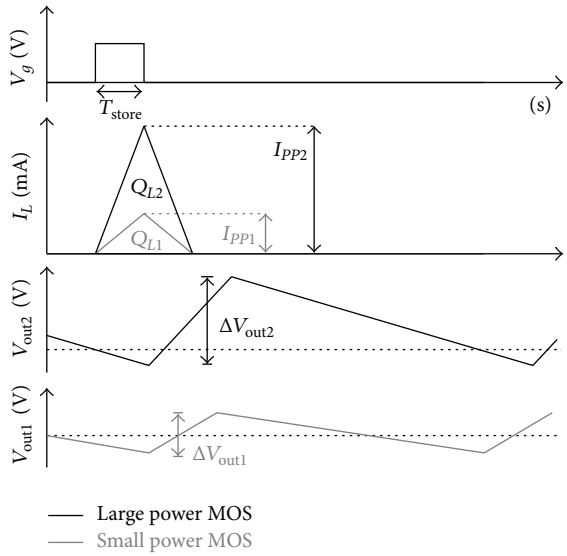

Figure 3: Analysis of inductor current and output voltage.

sleep modes, a little load current is required, and it is supplied by a small power MOS. In contrast, a large power MOS provides a large current when the load circuit is in the operating mode.

3.1. PFM Boost Converter in Light Load. If the boost converter in PFM mode is optimally designed for light load conditions, a small power MOS is used in the power stage. Since the peak inductor current I_{PP} is proportional to the size of the power MOS, so the stored energy Q_L in the inductor varies with the size of power MOS, as shown in Figure 3. As a result, the PFM boost converter with a small power MOS has a high power efficiency under light loads, but it cannot supply a large current for heavy loads as shown in Figure 4.

3.2. PFM Boost Converter in Heavy Load. When the PFM boost converter is designed for heavy loads, a large power MOS is needed to produce a large peak inductor current I_{PP2} and store much energy Q_{L2} in the inductor. Although a PFM boost converter with a large power MOS can provide large energy Q_L and has high power efficiency under heavy loads, its large conduction loss and leakage loss markedly degrade the power efficiency in light load currents, defeating the power-saving advantages of PFM in DCM operation, as shown in Figure 4. Additionally, a large output voltage ripple ΔV_{OUT2} seriously affects the circuit performance of the load system.

3.3. Proposed Parallel Power MOS. The size of the power MOS in the proposed PFM boost converter is accurately controlled

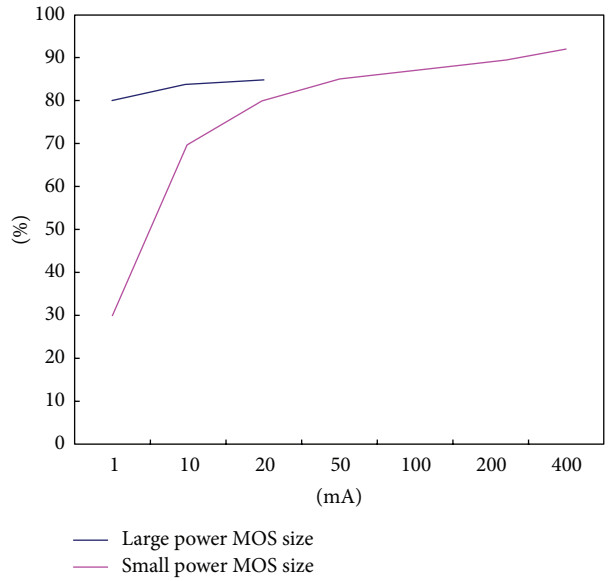

Figure 4: Power efficiency of different power MOS sizes.

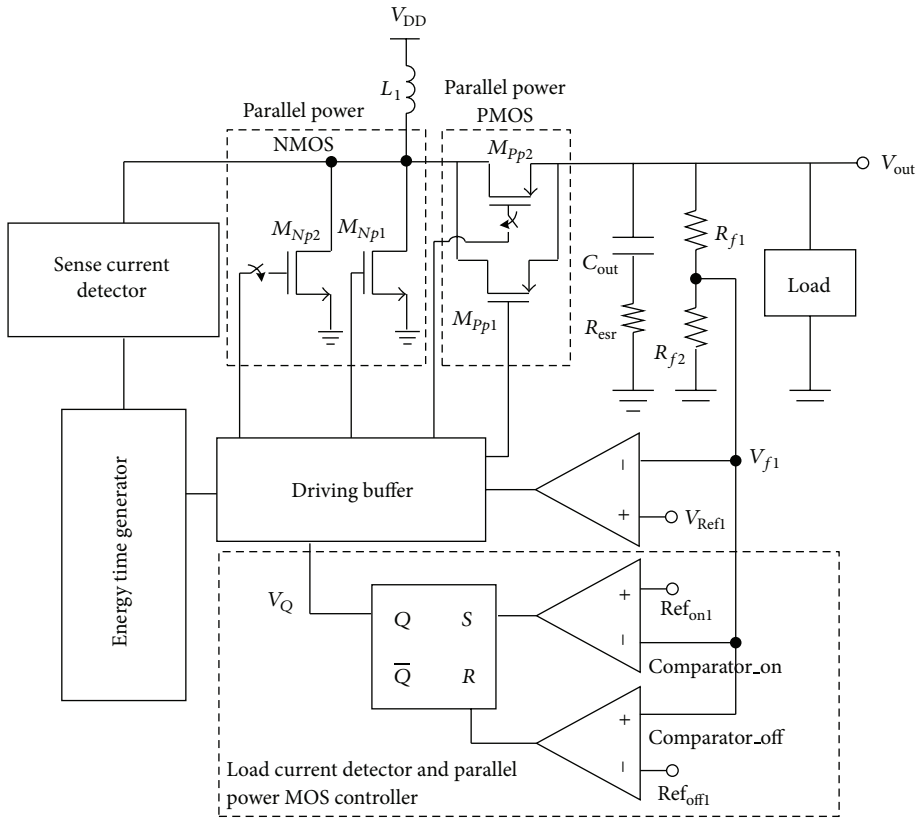

Figure 5: Proposed parallel power MOS controller and load current detector.

to yield high power efficiency from heavy load to light load. The parallel power MOS units are composed of the small power MOS M_{Pp1} and M_{Np1} and the large power MOS M_{Pp2} and M_{Np2}, which are displayed in Figure 5. When the boost converter operates under a heavy load, all power MOS units are operated to provide a large current to the load circuit. Furthermore, when the boost converter operates from heavy load to light load, the large power MOS units M_{Np2} and M_{Pp2} are turned off and the small power MOS units M_{Np1} and M_{Pp1} generate a small current to load circuits. Consequently,

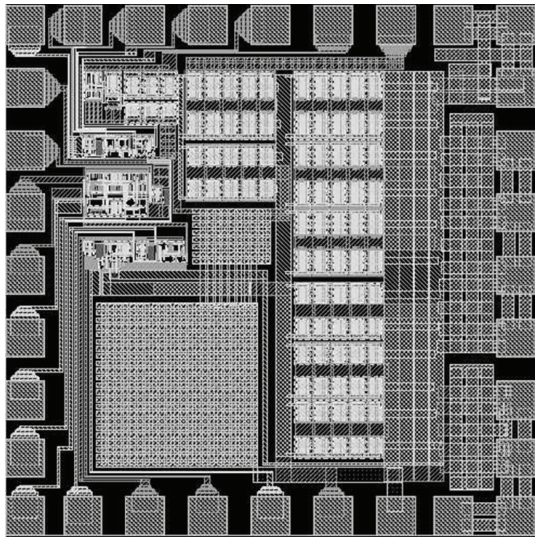

Figure 6: Die photograph of the proposed boost converter.

Table 1: Comparisons of dc-dc boost converters.

	[4]	[6]	Proposed
Control technique	PWM/PFM	PWM	PFM
Load current range	1 mA–600 mA	10 mA–150 mA	1 mA–420 mA
Power conversion efficiency	60%–92%	81%–95.5%	74.9%–90.74%
External compensated circuit	Yes	Yes	No
Chip area	Large	Large	Small

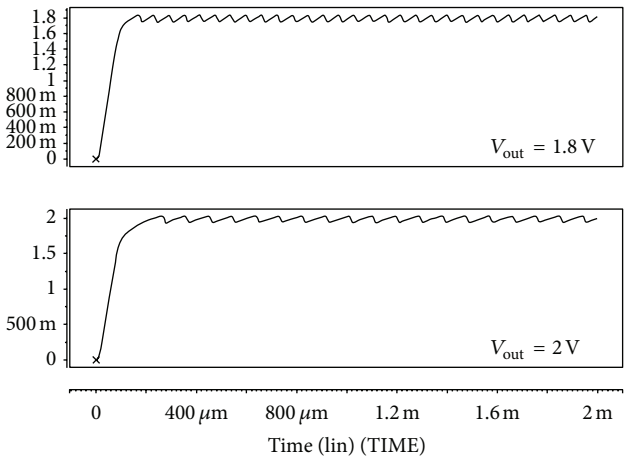

Figure 7: The boost converter boosts a 1.5 V supply to 1.8 V and 2 V at an output current of 420 mA.

the proposed circuit not only has high power efficiency under heavy loads but also maintains the advantages of PFM under light loads.

3.4. Proposed Parallel Power MOS Controller and Load Current Detector. Figure 5 schematically depicts the schematic of proposed parallel power MOS controller and load current detector, which consists of a hysteresis comparator_on, a comparator_Off, and an SR latch. When the converter operates at various load currents, the proposed circuit exactly detects variations of output voltage to determine the power MOS. The operational principle is described as follows. When the load current varies from light load to heavy load or the divider voltage V_f of the output voltage V_{out} is lower than the reference voltage Ref_{on1}, the output of comparator_ON sends a high signal through the SR latch to increase power MOS units. However, as the load current varies from heavy load to light load or the voltage V_f exceeds the reference voltage Ref_{off1}, the output of comparator_Off sends a high signal to reset the node of the SR latch to turn off the large power MOS M_{Pp2} and M_{Np2}. Furthermore, the SR latch not only controls the power MOS units but also hold the output signals of the comparator_on and comparator_Off. Thus, the power MOS units can be accurately determined by the proposed circuit.

4. Postlayout Simulation and Comparison Results

The proposed high-efficiency monolithic dc-dc boost converter is implemented using the TSMC 0.35 μm CMOS 2P4M technology. Figure 6 presents a die photograph of the proposed dc-dc PFM boost converter. The postlayout simulation results show that the proposed PFM boost converter can boost a 1.5 V supply to 1.8 V or 2 V at the 420 mA output current, as shown in Figure 7. Figure 8 shows the

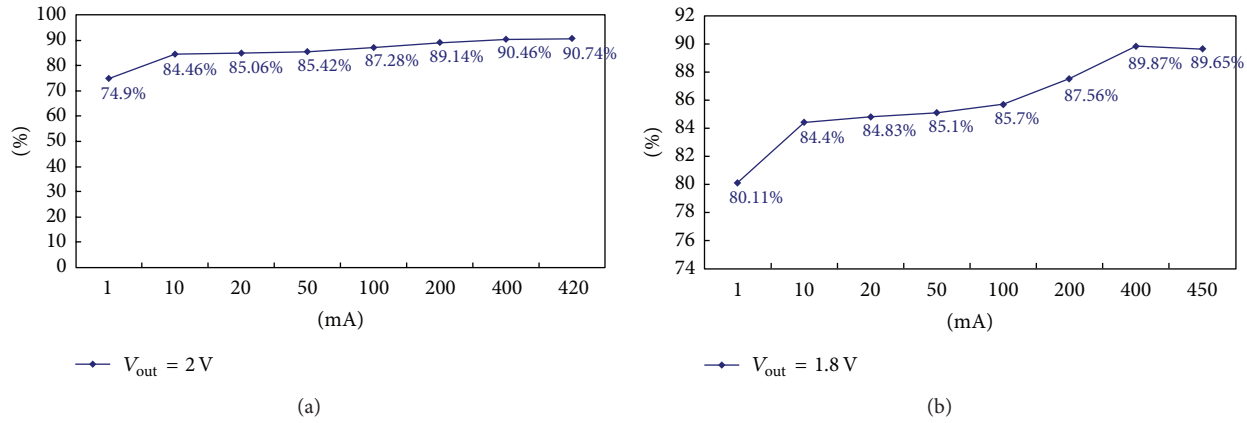

Figure 8: Power efficiency of the proposed PFM boost converter at (a) 1.8 V and (b) 2 V output voltages.

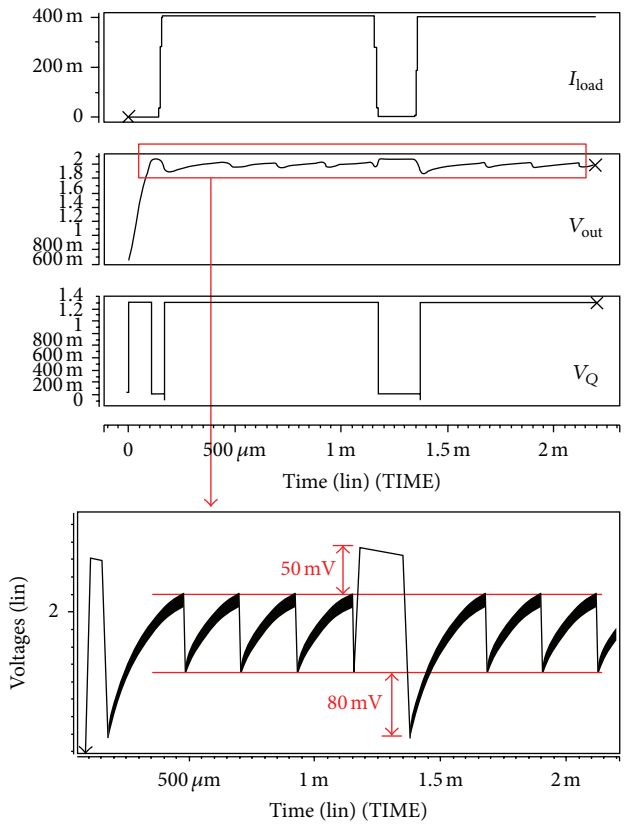

Figure 9: Transient response of the proposed boost converter under 400 mA load current step.

power efficiency of the proposed PFM boost converter at two supply voltages. The maximum power efficiency of the proposed converter exceeds 90.7% for 420 mA at 1.5 V supply. Figure 9 illustrates the transient response of the proposed boost converter when a 400 mA load current step is applied. As the load current varies from 1 mA to 400 mA, the load current detector detects a drop voltage 80 mV of output voltage and output voltage V_Q of the SR latch is changed to high to increase power MOS units. As the load decreases from 400 mA to 1 mA, a step voltage 50 mV of output voltage is detected units and voltage V_Q of the SR latch transmits a low signal to turn off the large power MOS M_{Pp2} and M_{Np2}. Additionally, when the boost converter is just started, the output voltage can be fast boosted to demand voltage even if small load current is needed as shown in Figure 9. The proposed circuit has a smaller chip area and a lower cost than other boost converters [4, 6], as indicated in Table 1, because the proposed circuit needs no PWM technique and external compensated circuit.

5. Conclusion

A high-efficiency dc-dc boost converter for a portable supply is designed with a standard CMOS process. The proposed boost converter verifies that the utilization of a parallel power MOS provides high power conversion efficiency from light load to heavy loads. The proposed load current detector and parallel power MOS controller accurately determines the size of power MOS under the different loads. The postlayout simulation results show that the power efficiency of the proposed circuit is 74.9% for a load current of 1 mA and 90.7% for a load current of 420 mA at a supply voltage of 1.5 V. Moreover, the area of the proposed circuit is smaller than those of the circuits in the literature under heavy to light loads. Thus, the proposed boost converter is very suitable for supplying power in modern portable devices.

Acknowledgments

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