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Low-complexity architecture of carrier frequency offset estimation and compensation for body area network systems

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ABSTRACT

This study presents a baseband communication architecture in compliance with IEEE 802.15.4 physical layer specifications for body area network systems. The proposed architecture uses preambles for a correlation operation to detect the front end of symbols and then calculates the influence of a channel effect, for example, a carrier frequency offset (CFO). Using a cross-correlation and auto-correlation architecture to synchronize receivers, the data subject to the carrier frequency can be compensated with a coordinate rotation digital computer (CORDIC) structure. This study includes a system simulation for the purpose of signal compensation in both the transmitting and receiving ends. Results show that the proposed design correctly detects the CFO bias in radians, with a detection error less than 0.1%, indicating that the CFO is compensated.

1. Introduction

An aging population and declining birth rate have caused a staffing shortage in health care. The elderly, and patients who suffer from chronic diseases and require long-term care, require long-term monitoring of physiological signals, including electrocardiograms (ECGs), cardiac index, body temperature (TE), blood pressure, cardiovascular status, and oxygen concentration, and so on. The equipment for acquiring these physiological signals can be further divided into small modules that can be operated independently, and are therefore suitable for home medical purposes. A number of studies have been carried out using a body area network (BAN) technique to transmit ECG measurements to hand-held mobile communication devices. The BAN technique also stores the measured data in a remote database through a mobile network [1–5]. The server can then perform a medical diagnosis and fulfill the application of a carry-care system.

BANs have been deployed rapidly around the world in recent years. The development of wireless consumer electronics for high accuracy transmission has made this a significant field of research. In compliance with IEEE 802.15.4, baseband digital signal processing (DSP) has been widely applied to BAN communications because of its high stability and validity [6–8]. As a spread signaling technique for communication over an independent identically distributed channel, the IEEE 802.15.4 physical layer is sensitive to the non-ideal front-end effect and imperfect synchronization. This often results in a carrier frequency offset (CFO) error. These CFO errors can significantly degrade the performance of the communication receiver. Previous studies have been conducted on the issue of CFO [9–14].

In the phase locked loop (PLL) method of CFO compensation [15], a phase locked loop-based frequency synthesizer (PLL-FS) consists of analog devices that are highly sensitive to ambient conditions such as temperature and humidity. The problems suffered by analog devices may lead to some unpredictable situations, and it may be difficult to regulate the frequency accordingly. The core part of a direct digital frequency synthesizer (DDFS) is essentially a fully digital design. Therefore, a DDFS can overcome the problems referred to above in the PLL-FS. A DDFS can be classified into two categories

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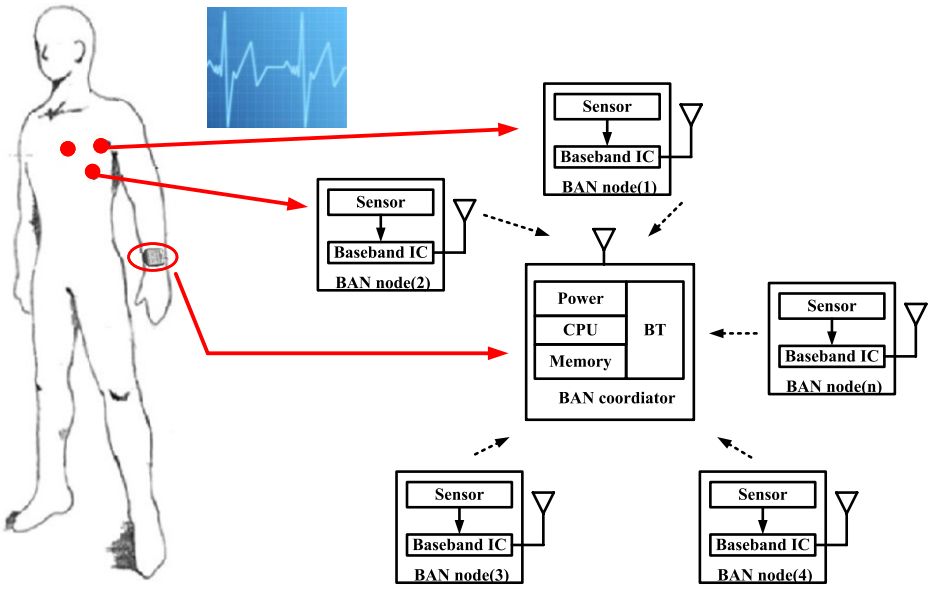

Fig. 1. A BAN transceiver.

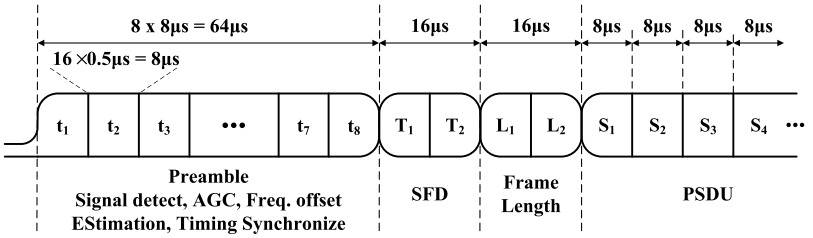

Fig. 2. The format of a PPDU.

depending on how it is implemented. The first is called the ROM-based DDFS implementation, while the second is called the coordinate rotation digital computer (CORDIC)-based DDFS implementation [16–20].

Raising the transmission accuracy as expected, the IEEE 802.15.4 physical layer procedure is sensitive to carrier frequency offset at a receiver. In an effort to solve this problem, the proposed architecture manages the frame and carrier synchronization with a precise digital oscillator and a re-modified multiplier. A CORDIC-based sinusoidal iterative generator, a divisor, and a frame controller assist with CFO compensation. This paper proposes a novel architecture and simple hardware design to realize the synchronization with CFO compensation. This design improves the CFO hardware architecture, and uses the CORDIC technique to increase accurate operation and the hardware simplifying technique to reduce hardware area. Implementation results show the performances of CORDIC and CFO compensation at different word-length numbers.

This paper is outlined as follows. Section 2 describes the system block diagram. Section 3 discusses the CFO compensation algorithm. Section 4 presents implementation results. Finally Section 5 draws conclusions.

2. The body area network system

In compliance with IEEE 802.15.4 physical specifications, this study proposes BAN baseband transmitting applied to an ECG monitoring IC. A low power intelligent sensor senses all the ECG signals at each BAN node, and then carries out baseband signal coding. In addition to an RF circuit, a BAN node module is formed and then transmits data in a star topology of BAN. Including a baseband receiving IC and an embedded system in the receiving end, the BAN coordinator module is combined with an embedded platform. Fig. 1 illustrates the whole system architecture. This study proposed a way to reduce the power dissipation during transmission, leading to a patient monitoring system with an extended life cycle.

As Fig. 2 shows, IEEE 802.15.4 stipulates the specification of a PHY protocol data unit (PPDU). It consists of three main parts: a synchronization header (SHR) including a preamble and a start-of-frame delimiter (SFD), a PHY header (PHR), and a PHY payload. The preamble field, composed of 32 bits of binary 0's, synchronizes the chip and a symbol upon receiving a package at the receiving end, where $t_1, \ldots, t_8$ denote a sequence of training symbols. Following the preamble field, an

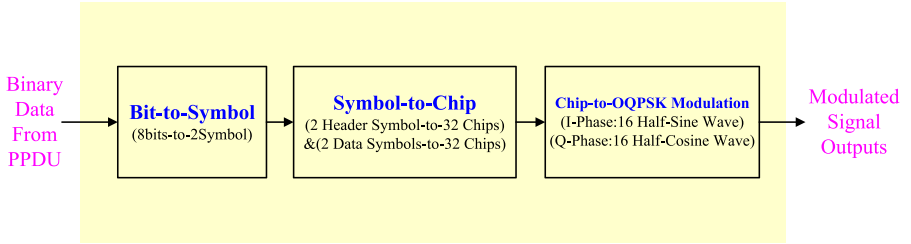

Fig. 3. Spreading functions in a baseband modulation.

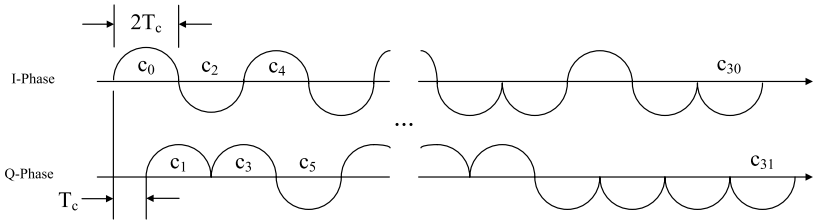

Fig. 4. Sample baseband chip sequences with pulse shaping.

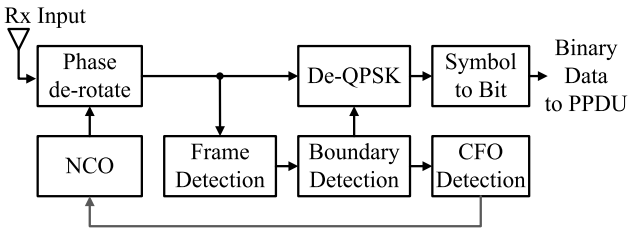

Fig. 5. A baseband receiver architecture.

SFD field marks the termination of the preamble field and the front end of the data package, specified as "1110_0101", an eight-bit binary datum, where both T_1 and T_2 denote boundary symbols. A frame length seven bits long specifies the byte length of a PHY service data unit (PSDU). In other words, the data must be confined within a length between 0 and 127. Therefore, the maximum value of the PSDU field is 127 bytes.

2.1. The transmitter

Fig. 3 shows that in the transmitter architecture of the IEEE 802.15.4 2.4 GHz physical layer, the data is transmitted in a serial fashion from the PPDU end to a bit-to-symbol circuit and converted into four-bit symbol signals. These signals are then mapped to 32-bit chip signals and modulated with the offset QPSK. Subsequently, a baseband spread encoder signal is transmitted. The data transmitted from BAN nodes consist of a two-byte header and a two-byte datum. The former ensures synchronization at the receiving end, while the latter represents the sensed physiological data.

The chip sequences representing each data symbol are modulated onto the carrier using O-QPSK with half-sine pulse shaping. Even-indexed chips are modulated onto an in-phase (I) carrier and odd-indexed chips are modulated onto a quadrature-phase (Q) carrier. Because each data symbol is represented as a 32-chip sequence, the chip rate (nominally 2.0 Mchip/s) is 32 times the symbol rate. To form the offset between the I-phase and the Q-phase chip modulations, the Q-phase chips lag behind the I-phase chips by T_c (Fig. 4), where T_c denotes the inverse of the chip rate.

2.2. The receiver

The block diagram of the receiver (Fig. 5) shows that it consists of three parts: package examination, carrier synchronization, and data recovery. Subsequent to a frame detection, following the preamble located at the forefront of the detection package, signals can be synchronized. It is also necessary to determine whether a carrier frequency shift has been sensed. The use of a numerically controlled oscillator (NCO) to turn the carrier phase shifting counterclockwise can compensate the data influenced by the carrier frequency shifting. After the shifting error is corrected and the signal passes all the way through de-QPSK, de-spread spectrum, and symbol-to-bit circuit, the transmitted data will be restored to the original form.

Because the carrier frequency of the oscillator in the transmitter does not match that in the receiver, a carrier frequency offset is induced inevitably. This degrades the orthogonality between carriers and causes phase rotation in the carrier

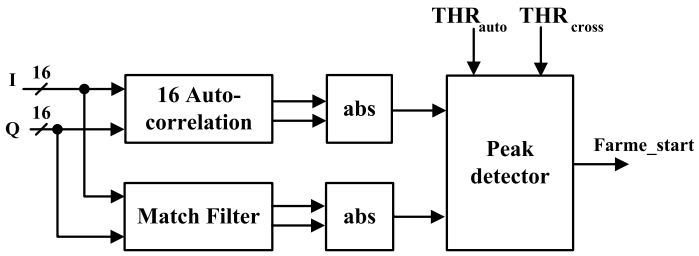

Fig. 6. A block diagram of frame detection.

frequency. In an effort to receive transmitted data precisely, the estimation and the compensation of such a non-ideal effect is highly critical. Because of noise interference in the channel, it is not possible to exactly estimate the amount of phase offset, meaning that it requires extra operations to calculate the residue phase error between the ideal and the estimated values. A number of synchronization circuits are required to resist the channel effect in the receiver.

3. Synchronization

In compliance with the IEEE 802.15.4 physical layer, this study presents a baseband made for the BAN synchronization with a preamble consisting of 32 bits of zeros in a channel affected by additive white Gaussian noise (AWGN) and a frequency rotation. Several features, including frame detection, boundary detection, CFO detection, and CFO compensation, are incorporated in a synchronization block diagram (Fig. 5).

3.1. Frame detection

The frame detection comprises an auto-correlation with a depth of 16 and a cross-correlation, referred to as a 16-tap match filter. To detect the peaks, the absolute value of the auto-correlation and the cross-correlation must be compared with respective thresholds, as shown in Fig. 6. Thus, auto-correlation plays a critical role in synchronization circuits.

The received signal correlates with a version of itself with one symbol delayed at the receiver. Let $A(n)$ denote the normalized auto-correlation, given as

$$A(n) = \frac{\sum_{k=0}^{15} r^*(n-k)r(n-k-16)}{\max\left(\sum_{k=0}^{15} r^*(n-k)r(n-k-16)\right)}, \tag{1}$$

where $r(n)$ denotes a received sequence, and the superscript * is a Hermitian operator. This study adopts an invariant threshold $THR_{auto} = 0.8$. Following the detection of the commencement of the frame, the receiver also utilizes a sliding correlator to correlate the received signal with the waveform of a known symbol in the preamble to find the symbol boundary and detect the preamble end time. This means that the so-called cross-correlation correlator functions as a match filter. Resulting in eight peaks, the 16-tap correlator is generated by the first known frame, given by

$$C(n) = \frac{\sum_{k=0}^{15} r(n-k)\cdot w^*(16-k)}{\max\left(\sum_{k=0}^{15} r(n-k)\cdot w^*(16-k)\right)}, \tag{2}$$

where $C(n)$ denotes the normalized cross-correlation at the time n, $w(k)$ is the coefficient weight value of the kth known sequence, and the coefficients $w(k), k = 0, 1, \ldots, 15$, are respectively defined as $[-1+j, 1+j, -1+j, -1-j, -1+j, -1-j, 1-j, 1-j, 1+j, -1-j, -1-j, 1+j, 1-j, -1+j, 1-j, 1+j]$.

3.2. CFO estimation and compensation

It is assumed that the transmission is made in an AWGN channel with a similar preamble symbol. The correlator performs maximum likelihood estimation (MLE) for CFO, and the preamble symbols are employed for CFO estimation in the IEEE 802.15.4 standard. Arbitrary kinds of successive preamble symbols can be used to perform the CFO radian operation as follows. To build a low-complexity architecture of the estimated CFO, a hardware implementation $\hat{\phi}$ is given as

$$\hat{\phi} = \frac{1}{2\pi}\arg\left(\sum_{k=0}^{15}\frac{r(n+k)\cdot w^*(16+k)}{Ns}\right), \tag{3}$$

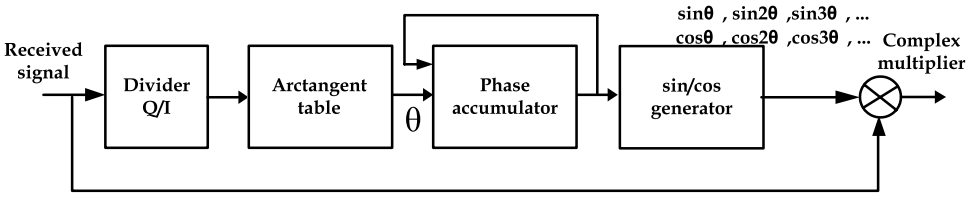

Fig. 7. A conventional ROM-based architecture for CFO estimation.

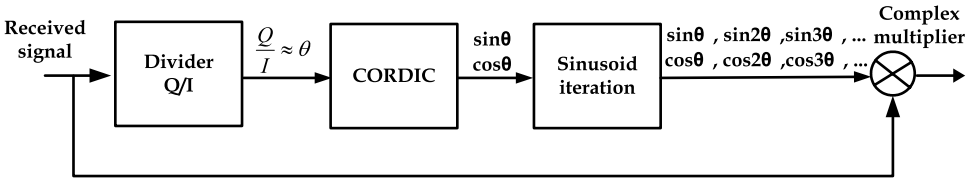

Fig. 8. A CORDIC-based sinusoid iteration oscillator for CFO estimation.

where arg(·) denotes the argument, $Ns = 16$ indicates preamble signals, and $r(n + k)$ denotes the received noisy output through the channel for the nth sample of the kth symbol.

The received data are retrieved by carrier frequency synchronization, given by

$$\hat{r}_k = r_k \cdot \exp(-j2\pi\hat{\phi}k), \tag{4}$$

where $r_k, k = 0, 1, 2, \ldots$, denote the complex signals at the outset of long symbols.

Fig. 7 show the conventional architecture of CFO estimation. Once we get the real and imaginary parts of output values of the auto-correlation, let the real part equal I and the imaginary part equal Q. It is then possible to calculate the tangent value by dividing Q by I. The rotated angle of CFO can be found from

$$\theta = \tan^{-1}\left(\frac{Q}{I}\right). \tag{5}$$

An arctangent look-up table is required to find the angle. If it is smaller than 0.5 rad, this angle can be approximated as

$$\frac{Q}{I} = \tan\theta \approx \theta, \quad \text{if } \theta < 0.5. \tag{6}$$

A 10% error rate is allowable in hardware implementation. Hence, theta is set to be less than 0.5 rad. When BER is less than 10^{-3}, the theta bias will be less than 0.5 rad.

After finding the rotated angle, an accumulator and a sin / cos generator are still required to perform the compensation. The generator is built to establish a sin / cos table whose size varies directly with precision. Rather than using a ROM, the proposed design adopts a CORDIC-based architecture described in the following subsections. However, a CORDIC requires multiple clock cycles to generate the intended sin / cos values, inefficiently reducing the chip area. For this reason, this study proposes the novel CFO estimation architecture depicted in Fig. 8.

3.3. The CORDIC algorithm

A CORDIC is used for multiplication, division, and hyperbolic functions. The CORDIC algorithm assumes that the rotation of a vector $[x_0, y_0]^T$ by an angle θ in Cartesian coordinates leads to a vector $[x_n, y_n]^T$, with the aid of matrix operations, computed as

$$\begin{bmatrix} x_n \\ y_n \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} = \frac{1}{\sqrt{1+\tan^2\theta}} \begin{bmatrix} 1 & -\tan\theta \\ \tan\theta & 1 \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix}. \tag{7}$$

Through specifications of the sign of σ_i, the given angle θ can be approximated as the sum of the partial angles α_i, that is,

$$\theta = \sum_{i=0}^{n-1} \sigma_i \alpha_i, \quad \sigma_i \in \{-1, 1\}. \tag{8}$$

The tangent function in Eq. (7) can be expanded into a power series in powers of 2 with the angle α_i. The accumulated partial angles z_i can be used to define the signs of the partial angles. For $z_0 = \theta$,

$$z_{i+1} = z_i - \sigma_i \tan^{-1}\left(2^{-i}\right), \quad \sigma_i = \begin{cases} +1 & z_i \geq 0 \\ -1 & z_i < 0, \end{cases} \tag{9}$$

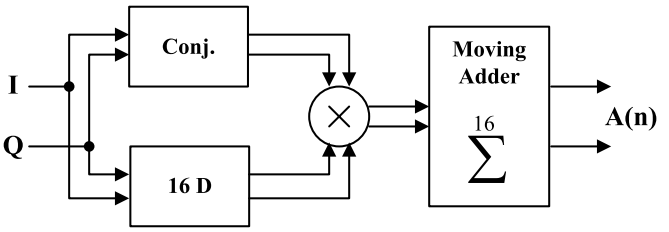

Fig. 9. An auto-correlation architecture.

Table 1
Weighting coefficient mapped to an adder function.

$w(k)$	$P(k)$	
	$P_I(k)$	$P_Q(k)$
$1+j$	$r_I(n-k)-r_Q(n-k)$	$r_I(n-k)+r_Q(n-k)$
$1-j$	$r_I(n-k)+r_Q(n-k)$	$-r_I(n-k)+r_Q(n-k)$
$-1+j$	$-r_I(n-k)-r_Q(n-k)$	$r_I(n-k)-r_Q(n-k)$
$-1-j$	$-r_I(n-k)+r_Q(n-k)$	$-r_I(i-k)-r_Q(n-k)$

where σ_i is the sense of rotation in the ith iteration. The matrix product of each step can be simplified into

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = k_i \begin{bmatrix} 1 & -\sigma_i 2^{-i} \\ \sigma_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x_i \\ y_i \end{bmatrix}, \quad k_i = \frac{1}{\sqrt{1+2^{-2i}}}. \tag{10}$$

A sinusoid iteration oscillator (SIO) replaces the conventional phase accumulator. Trigonometric functions, as in Eq. (11), are utilized to calculate the values of $\sin(k\theta)$ and $\cos(k\theta)$, where $k = 1, 2, 3, \ldots, N$, and N is the number of received signals. To address the iterative scheme, assume that $\varphi = \{0, \theta, 2\theta, 3\theta, \ldots (k-1)\theta\}$. The first rotated vectors, $\sin\theta$ and $\cos\theta$, can be computed by the CORDIC, and can be treated as the initial values of the SIO, as in Eq. (11):

$$\begin{aligned} \sin(\theta+\varphi) &= \sin\theta\cos\varphi + \cos\theta\sin\varphi \\ \cos(\theta+\varphi) &= \cos\theta\cos\varphi - \sin\theta\sin\varphi. \end{aligned} \tag{11}$$

Thus, the values of $\sin\theta$ and $\cos\theta$ can be viewed as given constants. For the sake of hardware architecture design, Eq. (11) is modified into

$$\begin{aligned} S_{i+1} &= S_o C_i + C_o S_i \\ C_{i+1} &= C_o C_i - S_o S_i, \end{aligned} \tag{12}$$

where $S_o = \sin\theta$, $C_o = \cos\theta$, $S_i = \sin\varphi$, and $C_i = \cos\varphi$. Because the SIO hardware design adopts the iteration structure, S_i and C_i represent the current state value and S_{i+1} and C_{i+1} represent the next state value. If $S_i = \sin 2\theta$ and $C_i = \cos 2\theta$, then $S_{i+1} = \sin\theta$ and $C_{i+1} = \cos 3\theta$.

4. The implementation result

As illustrated in Fig. 9, an auto-correlator with a depth of 16 consists of delay registers, a conjugate converter, a complex multiplier, and a moving adder. Hence, the output maintains the auto-correlation property. A match filter circuit, as demonstrated in Fig. 10, performs cross-correlation. Here, the received data are expressed as $r(n-k) = r_I(n-k)+jr_Q(n-k)$, where $k = (0, 1, 2, \ldots, 15)$, representing respective time delays. Since the preambles are the coefficients produced by QPSK, $w(k)$ can be defined as four constant complex numbers: $1+j$, $1-j$, $-1+j$, $-1-j$. However, the implementation of a correlator with such complex coefficients requires a costly and complex multiplier. Therefore, the required multiplication operations can be removed if the real and the imaginary parts of the correlator coefficients can be expressed as 2's complements together with the use of addition in the implementation. The first coefficient $w(0)$ is $-1+j$ (Fig. 10). As Table 1 shows, the output can be regarded as the output of the multiplier, that is, $P(0) = P_I(0) + jP_Q(0)$ and $P_I(0) = -r_I(n) - r_Q(n)$, $P_Q(0) = r_I(n) - r_Q(n)$.

Fig. 11 shows package frame synchronizations with an estimated position based on auto-correlation and cross-correlation operations with SNR = 10 dB.

The CFO estimations at the preambles employ both the real and the imaginary parts of the cross-correlation output. Fig. 12 shows the CFO estimation and compensation architecture. In an effort to reduce the chip area required, the adopted CFO estimation passes through the divisor and the CORDIC unit, which rotates the received signals.

A fixed-point number is a finite word-length representation of a corresponding floating-point number. A fixed-point number is a 2's complement consisting of a sign bit, three integer bits, and fractional bits. Fig. 13 shows the analysis of the

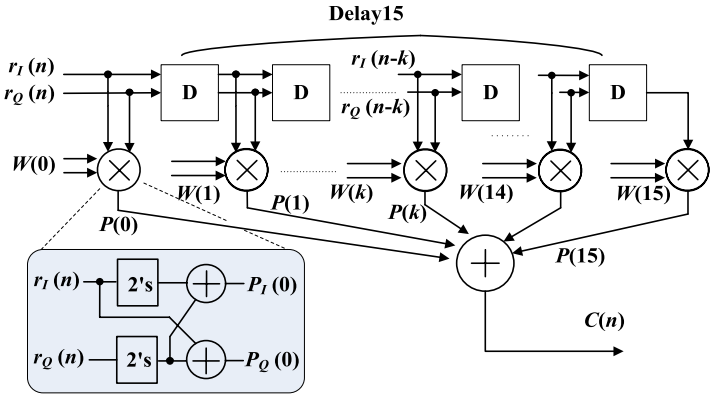

Fig. 10. A cross-correlation architecture.

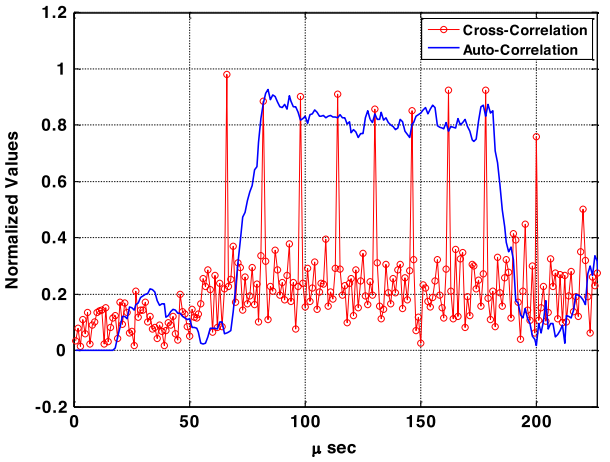

Fig. 11. Auto-correlation and cross-correlation detections.

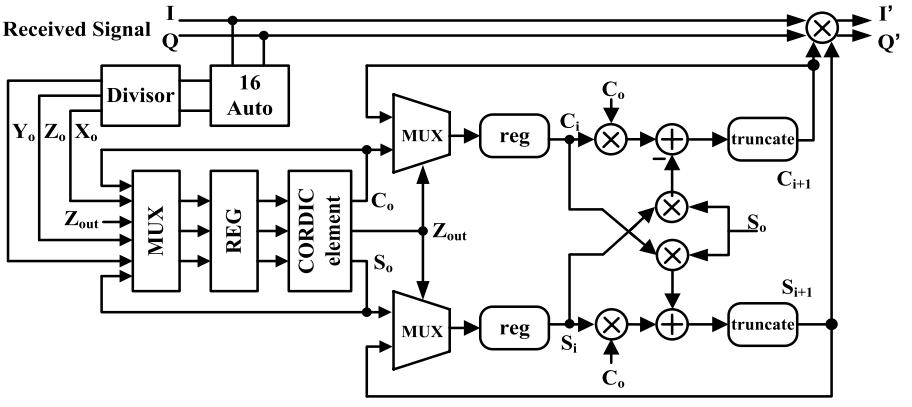

Fig. 12. A combinational circuit for the CFO estimation and compensation.

fractional word-length for hardware design. When the fractional word-length exceeds 10 bits, the CFO detection error will be reduced to 0.1% rad. Therefore, a fractional word-length of 10 bits is applied to all the buses of the CFO detector.

This study compares the simulation results in Fig. 14 with those of Karen et al. [7], who presented a MMSE receiver with training correlators but did not account for a carrier frequency offset. Short of phase error compensation in digital signal processing, an FPGA baseband solution also appears in [7]. In the current study, the simulation performance of the receiver with AWGN and CFO compensation is comparable to the case for AWGN only.

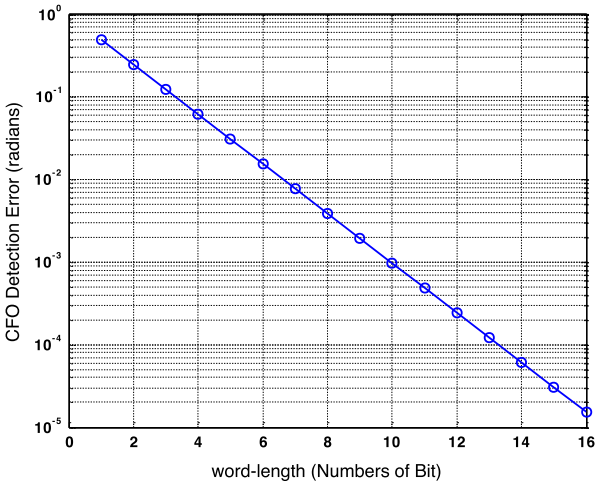

Fig. 13. An analysis on the fractional word-lengths.

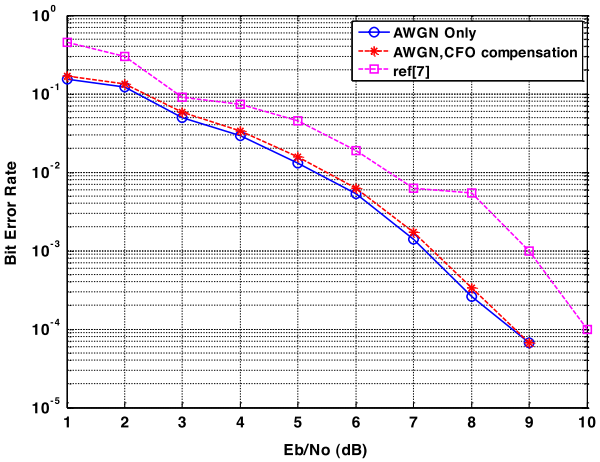

Fig. 14. A simulation for bit error rate versus E_b/N_0.

5. Conclusions

This study proposes a low-complexity baseband architecture for CFO estimation and compensation in BAN systems. In compliance with IEEE 802.15.4 physical layer specifications, a baseband architecture and a 2.4 GHz baseband transceiver are analyzed and characterized. To achieve the purpose of precise frame detection of received signals, this study uses CFO estimation and compensation for a system simulation and a hardware design. As an effective means to reduce the hardware complexity, digital logic and CORDIC circuits are built to implement correlation and radian operations, respectively. Results indicate that the signal performance, following CFO estimation and compensation, is comparable to that in the absence of CFO interference. The proposed design does not require a high bit resolution, and a fractional word length of 10 bits is long enough for hardware implementation.

Acknowledgments

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